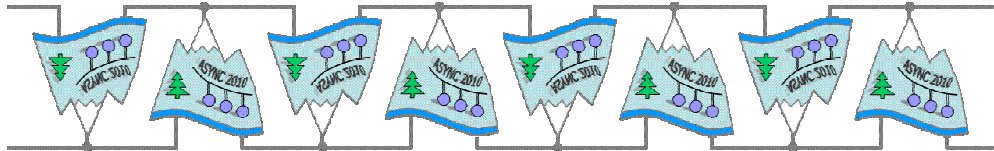




International Symposium on Networks-on-Chip

The 4th ACM/IEEE International Symposium on Networks-on-Chip



The 16th IEEE International Symposium on Asynchronous Circuits and Systems

ASYNC 2010 – NOCS 2010

3 – 6 May, 2010, Grenoble, France

Program Overview

Start time	Monday 3	Tuesday 4	Wednesday 5	Thursday 6	Friday 7	
9:00	Tutorials	Opening Session		Keynote 2, Pr. Keren Bergman <i>Photonic Interconnection Networks for Performance-Energy Optimized Computing</i>	Keynote 3, Dr. Alessandro Cremonesi <i>Semiconductor Industry: Perspective, Evolution and Challenges</i>	
9:30		Keynote 1, Pr. Mohamad Sawan <i>Low-power Bioelectronics for Massively Parallel Neuromonitoring</i>		Coffee Break	Coffee Break	
10:00						
10:30	Coffee Break	Coffee Break				
11:00	(Morning)	<i>Session ASYNCA1</i> Logic and Physical Synthesis	<i>Session NOCS N1</i> Flow Control and Routing	<i>Session ASYNC A4</i> Low-power and Harvesting	<i>Session NOCS N4</i> Memory and Efficiency	
11:30				<i>Session ASYNC A7</i> Power-Performance Optimisation	<i>Session NOCS N7</i> Topology and Architectures	
12:00						
12:30	Lunch	Lunch	Lunch	Lunch	Touring in Grenoble Area 9:00 18:00	
13:30						
14:00	Tutorials	<i>Common Session ASYNC-NOCS NA2</i> GALS-Based NoC Design		<i>Common Session ASYNC-NOCS AN5</i> Synchronizers		<i>Common Session ASYNC-NOCS NA8</i> Emerging Technologies
14:30						
15:00			Coffee Break	Coffee Break		
15:30	Coffee Break	Coffee Break				
16:00	(Afternoon)	<i>Embedded Invited ASYNC Session A3</i> Startups in Async. Design	<i>Session NOCS N3</i> Router Design	<i>Session ASYNC A6</i> High Level Synthesis and Retiming		<i>Session NOCS N6</i> Application-Driven Optimization
16:30				<i>Session ASYNC A9</i> Arbitration, Delay-insensitivity, GasP		<i>Session NOCS N9</i> Traffic Modeling and Management
17:00						
17:30		Poster Session 1		Poster Session 2 Demonstration Session		Poster Session 3
17:30					Closing Session - Best Paper	
18:00						
18:30						
19:00	Welcome Reception		Gala Dinner <i>"The Bastille"</i>			
22:00						

Monday, May 3, 2010, Tutorials

For our common ASYNC-NOCS 2010 tutorials, we are pleased to present this year 3 full tracks with full-day and half-day tutorials. The program contains 2 tutorials covering NoC topics, and 3 tutorials covering Async topics.

Most of the tutorials will include both **theoretical aspects** and some challenging **practical work**. The participants will have the exciting opportunity to do some **real lab exercises** on computers, using participant's laptops or desktop computers.

The tutorials will take place in the laboratories of the **CIME facilities** (*Centre Interuniversitaire de MicroElectronique et Nanotechnologies*), see <http://www.cime.inpg.fr/>, which is located just nearby the MINATEC building.

Tutorial N1 9:00 – 12:30	Tutorial N2 9:00 – 12:30	Tutorial A2 9:00 – 12:30
<p><i>Virtual Prototyping of NoC-based MPSoC: Fundamentals & Case Studies</i> (Part I)</p> <p>Alain Greiner (UPMC/LIP6), Nicolas Pouillon (UPMC/LIP6), Frédéric Pétrot (INPG/TIMA), Fabien Colas-Bigey (Thales), Laurent Maillet-Contoz (STMicro), Nguyen Huy-Nam (Bull).</p>	<p><i>Dynamic Power Management of Multi-Core Systems Under Workload- and Technology-driven Variations</i></p> <p>Radu Marculescu (Carnegie Mellon Univ) Umit Y. Ogras (Intel Corp).</p>	<p><i>A Simulation Tool for the Study of Metastability in SoCs</i></p> <p>Tom Chaney (Blendics LLC), Dave Zar (Univ. Washington).</p>
Room: CIME	Room Minatec, 222+223+224	Room : CIME
Lunch, 12:30 – 14:00		
Tutorial N1 14:00 – 17:30	Tutorial A1 14:00 – 17:30	Tutorial A3 14:00 – 17:30
<p><i>Virtual Prototyping of NoC-based MPSoC: Fundamentals & Case Studies</i> (Part II)</p>	<p><i>ASIPIDE: a graphical framework to design and debug GALS systems through simulation and prototyping</i></p> <p>Lilian Janin (Univ. Manchester), Shoujie Li (Univ. Manchester), Doug Edwards (U. Manchester).</p>	<p><i>AHMOSE: Asynchronous High-speed Modeling and Optimization Tool-set</i></p> <p>Eslam Yahya (INPG/TIMA), Jeremie Hamon(INPG/TIMA), Laurent Fesquet (INPG/TIMA).</p>
Room: CIME	Room : CIME	Room : CIME

- During the tutorials, there will morning (10:30-11:00) and afternoon (15:30-16:00) coffee breaks. All coffee breaks will take place in the MINATEC Grand Salon.

Monday, May 3, 2010, Welcome Reception

19:00 – 22:00
ASYNC 2010 – NOCS 2010 - <i>Welcome Reception</i>
Room : MINATEC Grand Salon

Tuesday, May 4, 2010 (Morning)

9:00 – 9:30, Auditorium	
ASync 2010 - NOCS 2010 <i>Opening Session</i>	
9:30 – 10:30, Auditorium	
1 st Keynote Low-power Bioelectronics for Massively Parallel Neuromonitoring <i>Pr. Mohamad Sawan</i> , University of Montreal Session Chair : Rajit Manohar, Cornell Univ.	
10:30 – 11:00, Coffee Break	
11:00 – 12:30, Small Hall	11:00 – 12:30, Auditorium
ASync	NOCS
<p>Session A1 : Logic and Physical Synthesis Chair : Steven Nowick, Columbia University 11:00-11:30 Click Elements, An Implementation Style for Data-driven Compilation <i>Ad Peeters¹, Frank te Beest¹, Mark de Wit¹ and Willem Mallor²</i> ¹Philips, ²NXP 11:30-12:00 M-of-N Code Decomposition for Indicating Combinational Logic, <i>William Toms, Doug Edwards</i> University of Manchester 12:00-12:30 Concurrency Reduction of Untimed Latch Protocols - Theory and Practice <i>Santosh Varanas¹, Kenneth Stevens¹ and Graham Birtwistle²</i> ¹University of Utah, ²University of Sheffield</p>	<p>Session N1 : Flow Control and Routing Chair: Yvain Thonnart, CEA LETI 11:00-11:30 Evaluating Bufferless Flow-Control for On-Chip Networks <i>George Michelogiannakis and Daniel Sanchez</i> Stanford University 11:30-12:00 Comparison of Deadlock Recovery and Avoidance Mechanisms to Approach Message Dependent Deadlocks in On-Chip Networks <i>Andreas Lankes¹, Thomas Wild¹, Soeren Sonntag², Helmut Reinig³, Andreas Herkersdorf¹</i> ¹Technische Universität München, ²Lantiq Deutschland GmbH, ³Infineon Technologies AG 12:00-12:30 Addressing Manufacturing Challenges with Cost-Efficient Fault Tolerant Routing <i>Samuel Rodrigo¹, José Flich¹, Antonio Roca¹, Simone Medardoni², Davide Bertozzi², Jesús Camacho¹, Federico Silla¹, José Duato¹</i> ¹Universidad Politécnica de Valencia, ²Università di Ferrara</p>
12:30 – 14:00, Lunch	

Tuesday, May 4, 2010 (Afternoon)

14:00 – 15:30, Auditorium		ASYNC – NOCS Common Session		
<p>Session NA2 : GALS-Based NoC Design Chair: Davide Bertozzi, Univ. of Ferrara 14:00-14:30 Improving the Performance of GALS-Based NoCs in the Presence of Process Variation <i>Carles Hernández, Antoni Roca, Federico Silla, Jose Flich, Jose Duato</i> Universidad Politécnica de Valencia 14:30-15:00 A Low-Overhead Asynchronous Interconnection Network for GALS Chip Multiprocessors <i>Michael N. Horak¹, Steven M. Nowick², Matthew Carlberg³, Uzi Vishkin⁴</i> ¹Advanced Simulation Technology, Inc., ²Columbia University, ³UC Berkeley, ⁴University of Maryland 15:00-15:30 Asynchronous Bypass Channels : Improving Performance for DVFS and GALS NoCs <i>Tushar Jain, Paul Gratz, Alex Sprintson, Gwan Choi</i> Texas A&M University</p>				
15:30 – 16:00, <i>Coffee Break</i>				
16:00 – 17:30, Small Hall		ASYNC	16:00 – 17:30, Auditorium	
NOCS		<p>Session N3 : Router Design Chair: Jose Flich, Universidad Politecnica de Valencia 16:00-16:30 Ultra Fine-Grained Run-Time Power Gating of On-Chip Routers for CMPs <i>Hiroki Matsutan¹, Michihiro Koibuchi², Daisuke Ikebuchi³, Kimiyoshi Usami⁴, Hiroshi Nakamura¹, Hideharu Amano³</i> ¹The University of Tokyo, ²National Institute of Informatics, ³Keio University, ⁴Shibaura Institute of Technology 16:30-17:00 Design of a High-Throughput Distributed Shared-Buffer NoC Router <i>Rohit Sunkam Ramanujam¹, Vassos Soteriou², Bill Lin¹, Li-Shiuan Peh³</i> ¹University of California, San Diego, ²Cyprus University of Technology, ³Princeton University 17:00-17:15 Soft-Error Handling in On-Chip Networks <i>Young Hoon Kang, Taek-Jun Kwon, Jeff Draper</i> Univ. of Southern California/Information Sciences Institute 17:15-17:30 A 128x128x20Gbp/s Crossbar, Interconnecting 128 Tiles in a Single Hop, and Occupying Less than 5% of Their Area Giorgos Passas, Manolis Katevenis, Dionisis Pnevmatikatos FORTH-ICS, GREECE</p>		
<p>Session A3 : Embedded Invited Session: Start-ups in Asynchronous Design Chair: Alex Yakovlev, Newcastle Univ. 16:00-17:00 Proteus: Demonstrating Automated Design of GHz Asynchronous Circuits through a High-Density Next-Generation Low-Latency Ethernet Switch Chip <i>Peter A. Beerel and Georgios D. Dimou,</i> Timeless Design Automation <i>Andrew M. Lines,</i> Fulcrum Microsystems</p>				
17:30 – 18:30 : ASYNC – NOCS Poster Session (Posters of Tuesday presentations)				

Wednesday, May 5, 2010 (Morning)

9:00 – 10:00, Auditorium	
2 nd Keynote Photonic Chip-Scale Interconnection Networks for Performance-Energy Optimized Computing <i>Pr. Keren Bergman</i> , Columbia University Session Chair : Ran Ginosar, Technion	
10:00 – 10:30, Coffee Break	
10:30 – 12:00, Small Hall	10:30 – 12:00, Auditorium
ASync	NOCS
Session A4 : Low-power and Harvesting Chair : Laurent Fesquet , TIMA 10:30-11:00 Minimum-Energy Sub-Threshold Self-Timed Circuits: Design Methodology and a Case Study <i>Omer Can Akgun¹, Joachim Rodrigues¹ and Jens Sparsø²</i> ¹ Lund University, ² Technical University of Denmark 11:00-11:30 Static Power Reduction Techniques for Asynchronous Circuits <i>Carlos Otero, Jonathan Tse and Rajit Manohar</i> Cornell University 11:30-12:00 Bringing Robustness and Power Efficiency to Autonomous Energy Harvesting Microsystems <i>Jean-Frederic Christmann¹, Edith Beigne¹, Cyril Condemine¹, Pascal Vivet¹, Guy Waltisperger¹, Jerome Willemin¹ and Nicolas Leblond²</i> ¹ CEA-LETI, ² TIEMPO SAS	Session N4 : Memory and Efficiency Chair: Sungjoo Yoo , Postech 10:30-11:00 A Low-Latency and Memory-Efficient On-Chip Network <i>Masoud Daneshtalab, Masoumeh Ebrahimi, Hannu Tenhunen</i> University of Turku 11:00-11:30 Temperature-Aware Delay Borrowing for Energy-Efficient Low-Voltage Link Design <i>David Wolpert, Bo Fu, Paul Ampadu</i> University of Rochester, Rochester, NY USA 11:30-12:00 Comparing Energy and Latency of Asynchronous and Synchronous NoCs for Embedded SoCs <i>Daniel Gebhardt, Junbok You, Kenneth Stevens</i> University of Utah
12:00 – 13:30, Lunch	

Wednesday, May 5, 2010 (Afternoon)

13:30 – 15:00, Auditorium		ASYNC – NOCS Common Session	
Session AN5 : Synchronizers Chair : Mark Greenstreet , University of British Columbia 13:30-14:00 The Even/Odd Synchronizer: A Fast, All-Digital, Periodic Synchronizer <i>William Dally^{1,2} and Stephen Tell²</i> ¹ NVIDIA, ² Stanford University 14:00-14:30 Extending Synchronization from Super-threshold to Sub-threshold Region <i>Jun Zhou¹, Maryam Ashouei¹, David Kinniment², Jos Huisken¹ and Gordon Russell²</i> ¹ IMEC Netherlands, ² Newcaslte University 14:30-15:00 The Devolution of Synchronizers <i>Salomon Michel Beer, Ran Ginosar, Ruven Dobkin and Avinoam Kolodny</i> Technion			
15:00 – 15:30, Coffee Break			
15:30 – 17:00, Small Hall		15:30 – 17:00, Auditorium	
ASYNC		NOCS	
Session A6 : High Level Synthesis and Retiming Chair : Erik Brunvand , Univ. of Utah, USA 15:30-16:00 A fast branch-and-bound approach to asynchronous high-level synthesis <i>John Hansen and Montek Singh</i> UNC Chapel Hill 16:00-16:30 Automated Microarchitectural Exploration for Achieving Throughput Targets in Pipelined Asynchronous Systems <i>Gennette Gill and Montek Singh</i> UNC Chapel Hill 16:30-17:00 Improving Synchronous Elastic Circuits: Token Cages and Half-Buffer Retiming <i>Mario R. Casu</i> Politecnico di Torino		Session N6 : Application-Driven Optimization Chair: Federico Angiolini , iNoCs 15:30-16:00 Physical-Aware Link Allocation and Route Assignment for Chip Multiprocessing <i>Nikita Nikitin¹, Satrajit Chatterjee², Jordi Cortadella¹, Michael Kishinevsky², Umit Ogras²</i> ¹ Universitat Politecnica de Catalunya, ² Intel Corporation 16:00-16:30 Network-on-Chip Architectures for Neural Networks <i>Dmitri Vainbrand and Ran Ginosar</i> Technion, Israel 16:30-16:45 Transient and Permanent Error Co-Management Method for Reliable Networks-on-Chip <i>Qiaoyan Yu, Rabeeh Majidi, Paul Ampadu</i> University of Rochester 16:45-17:00 Back Suction: Service Guarantees for Latency-Sensitive On-Chip Networks <i>Jonas Diemer and Rolf Ernst</i> IDA, TU Braunschweig, Germany	
17:00 – 18:30		ASYNC – NOCS Poster Session (<i>Posters of Wednesday presentations</i>) ASYNC – NOCS Demonstration Session (<i>See list of Demos on the Web Site</i>)	
19:00 – 23:30 Gala Dinner at "The Bastille"			

Thursday, May 6, 2010 (Morning)

9:00 – 10:00, Auditorium	
<p>3rd Keynote</p> <p>Semiconductor Industry: Perspective, Evolution and Challenges</p> <p>Dr. Alessandro Cremonesi – STMicroelectronics</p> <p>Session Chair : Ahmed Jerraya, CEA LETI</p>	
10:00 – 10:30, Coffee Break	
10:30 – 12:00, Small Hall	10:30 – 12:00, Auditorium
ASync	NOCS
<p>Session A7 : Power-Performance Optimisation</p> <p>Chair : Montek Singh, UNC Chapel Hill</p> <p>10:30-11:00</p> <p>An Asynchronous FPGA with Two-Phase Enable-Scaled Routing</p> <p><i>Christopher LaFrieda, Benjamin Hill and Rajit Manohar</i></p> <p>Cornell University</p> <p>11:00-11:30</p> <p>An Operand-Optimized Asynchronous IEEE-754 Double-Precision Floating-Point Adder</p> <p><i>Basit Riaz Sheikh and Rajit Manohar</i></p> <p>Cornell University</p>	<p>Session N7 : Topology and Architectures</p> <p>Chair: Paul Ampadu, Univ. of Rochester</p> <p>10:30-11:00</p> <p>Improved Utilization of NoC Channel Bandwidth by Switch Replication for Cost-Effective Multi-Processor Systems-on-Chip</p> <p><i>Medardoni Simone¹, Francisco Gilabert², Maria Engracia Gomez², Davide Bertozzi¹</i></p> <p>¹University of Ferrara, ²Universidad Politecnica de Valencia</p> <p>11:00-11:30</p> <p>Physical vs. Virtual Express Topologies with Low-Swing Links for Future Many-core NoCs</p> <p><i>Chia-Hsin Owen Chen¹, Niket Agarwal², Tushar Krishna¹, Li-Shiuan Peh¹</i></p> <p>¹MIT, ²Princeton University</p> <p>11:30-11:45</p> <p>Design of High-Radix Clos Network on Chip</p> <p><i>Yu-Hsiang Kao, Najla Alfaraj, Ming Yang, H. Jonathan Chao</i></p> <p>Polytechnic Institute of New York University</p> <p>11:45-12:00</p> <p>Hierarchical Network-on-Chip for Embedded Many-Core Architectures</p> <p><i>Alexandre Guerre¹, Nicolas Ventroux¹, Raphaël David¹, Alain Mériçot²</i></p> <p>¹CEA LIST, ²IEF, Université Paris Sud</p>
12:00 – 13:30, Lunch	

Thursday, May 6, 2010 (Afternoon)

13:30 – 15:00, Auditorium		ASYNc – NOCS Common Session	
<p>Session NA8 : Emerging Technologies Chair: Radu Marculescu, Carnegie Mellon University 13:30-14:00 A Low-Cost Deadlock-Free Design of Minimal-Table Rerouted XY-Routing for Wireless NoCs <i>Ruizhe Wu¹, Yi Wang¹, Danella Zhao¹, Takamaro Kikkawa²</i> ¹University of Louisiana at Lafayette, ²Hiroshima University 14:00-14:30 Power-Efficient and High-Performance Multi-Level Hybrid Nanophotonic Interconnect for Multicores <i>Randy Morris and Avinash Kodi</i> Ohio University 14:30-14:45 Performance Evaluation of a Multicore System with Optically Connected Memory Modules <i>Paul Vincent Meija¹, Rajeevan Amirtharajah¹, Matthew Farrens², Venkatesh Akella¹</i> ¹Department of Electrical and Computer Engineering, University of California, Davis, ²Department of Computer Science, University of California, Davis 14:45-15:00 Traffic- and Thermal-Aware Run-Time Thermal Management Scheme for 3D NoC Systems <i>Chih-Hao Chao, Kai-Yuan Jheng, Hao-Yu Wang, Jia-Cheng Wu, An-Yeu Wu</i> National Taiwan University</p>			
15:00 – 15:30, Coffee Break			
15:30 – 17:00, Small Hall		15:30 – 17:00, Auditorium	
ASYNc		NOCS	
<p>Session A9 : Arbitration, Delay-Insensitivity, GasP Chair : Jens Sparsø, DTU 15:30-16:00 Formal Verification of an Arbiter Circuit <i>Chao Yan, Mark Greenstreet and Jochen Eisinger</i> University of British Columbia 16:00-16:30 Delay insensitivity does not mean slope insensitivity! <i>Florent Ouchet, Laurent Fesquet and Katell Morin-Allory</i> TIMA (Grenoble INP - UJF - CNRS) 16:30-17:00 Long-Range GasP with Charge Relaxation <i>Swetha Mettala Gilla, Marly Roncken and Ivan Sutherland</i> Portland State University</p>		<p>Session N9 : Traffic Modeling and Management Chair: Ran Ginosar, Technion 15:30-16:00 Distributed Sequencing for Resource Sharing in Multi-Applicative Heterogeneous NoC Platforms <i>Yvain Thonnart, Romain Lemaire, Fabien Clermidy</i> CEA, LETI, MINATEC 16:00-16:30 QuaLe: A Quantum-Leap Inspired Model for Non-Stationary Analysis of NoC Traffic in Multi-Processor Platforms <i>Paul Bogdan, Miray Kas, Radu Marculescu, Onur Mutlu</i> Carnegie Mellon University 16:30-16:45 Impact of Half-Duplex and Full-Duplex DMA Implementations on NoC Performance <i>F. Palumbo, Danilo Pani, Alessandro Pilia, Luigi Raffo</i> Dept. of Electrical and Electronic Engineering, Univ. of Cagliari 16:45-17:00 A Network Congestion-Aware Memory Controller <i>Dongki Kim, Sungjoo Yoo, Sunggu Lee</i> POSTECH</p>	
17:00 – 17:30		17:00 – 17:30	
ASYNc – NOCS Poster Session		(Posters of Thursday presentations)	
17:30 – 18:00		Closing Session and Best paper Awards	

Friday, May 7, 2010

On Friday 7th May will be organized a full day touring in the Grenoble area. The program will be the following : visit of the Grenoble downtown and historical center with a guide in the morning, a nice lunch in a Grenoble typical restaurant, and in the afternoon visit of the Chartreuse monastery (http://www.chartreuse.fr/pa_corriere_gb.htm), with a final visit of the Voiron Cave (http://www.chartreuse.fr/pa_sommaire_uk.htm) where are produced liquors by monastery monks.

This will be a unique opportunity to have a real Grenoble area experience, and to have an extra day in Grenoble to share with conference participants!

The organizers reserve the right of cancel the visit in case the number of participants is too low. In that case, reimbursement of the registered participants will be done.

Saturday, May 8, 2010

For people who would like to take advantage of their stay in Grenoble and would really like to enjoy mountain walking in nearby Grenoble Mountains, we propose to organize a one day mountain walking on Saturday 8 May. The idea would be to organize this as a costless event, self organized using our own cars, and we would share the picnic together.

For this, please contact: Cedric Koch-Hofer, (email: cedric.koch-hofer@cea.fr)

According to the number of people we are, and also according to the Saturday weather, various hiking solutions are possible in the close area : Vercors Moucherotte, Belledonne and Chamrousse, Chartreuse Dent de Crolles, ...

Do not hesitate to join us ! and do not forget to bring the appropriate shoes and pans.