Long-Range GasP with Charge Relaxation

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ASYNC, 6 May 2010
Title: TECOTOSH
TEnsion + COmpression + TOrsion + SHear

Location: Maseeh College
Installed: March 2006.
Dimensions: 130' x 40' x 40'.
Materials: Stainless steel truss, laminated dichroic glass, stainless steel cables and hardware. Aluminum light housings.

Engineers:
Bob Grummel and Grant Davis.
Project Manager: Oanh Tran.
Introduction

2008 Infinity chip (90nm CMOS by TSMC):
- 10% degradation of peak throughput
- for 5000 versus 500 lambda long interconnect
  - \( \lambda = 50 \text{ nm} \)
  - and so: 5000 \( \lambda = 0.25 \text{ mm} \)

First wire delay study (Prasad Joshi – USC):
- Logical Effort + Lumped Capacitance model
- confirms measured observations
- inadequate for wires above 5000 \( \lambda \)
Introduction (2)

Second wire delay study (Swetha – PSU):
  • uses Distributed RC model for interconnect
  • distinguishes voltage levels at both wire ends

Distinguishing both wire ends matters!
  • The two ends play a different role
    in single-track handshake signaling
    • NEAR-END: starts and stops the forward drive
    • FAR-END: starts and stops the reverse drive
  • True for ALL single-track signaling methods
## Introduction (3):
### Faith versus Measurement

<table>
<thead>
<tr>
<th>Single-Track Handshake</th>
<th>Multi-Track Handshake</th>
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**Single-Track Handshake**
- Drive high
- Drive low
- Faith

**Multi-Track Handshake**
- Uses FAITH in engineering and tools

- Drive high
- Drive low
- Faith
- Time
### Introduction (3):

**Faith versus Measurement**

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**Single-Track Handshake**

- Faith

**Multi-Track Handshake**

- Measuremen

| Uses FAITH in engineering and tools | Uses MEASUREMENT built into the design |

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Introduction (4)
Putting Things in Perspective

**FAITH versus MEASUREMENT** is everywhere
- Designs usually have a bit of both
  - Examples of Faith: isochronic fork, bundled-data
  - Examples of Measurement: 1-of-N data

Our Goal:
- Test the limits of FAITH in single-track handshaking

Scope:
- GasP is the study target
- But the results apply also to other single-track families
Introduction (5): Take-Away

Distance Constraint Graph

0 10k 20k 30k 40k

FAIL

Predecessor Wire Length

Successor Wire Length

Relaxation

Driven

CL

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Introduction (5): Take-Away

The amount of **CHARGE** matters

*NOT* the amount of **TIME**
Outline

• GasP design
• Simulation Experiments
  • Set-up
  • Delay-Voltage waveforms
  • Throughput results
• Wire engineering
• Summary
6-4 GasP
Cycle time: 6 gates FORWARD + 4 gates REVERSE = 10
Simulation Set-Up

- FIFO ring with ten 6-4 GasP modules
  - 3 R-C-R sections per 1000 lambda of the "long wire"
- Simulations
  - Forward and reverse delays: $SUCC_{10}$ to/from $PRED_1$
  - Voltage levels at the two ends: $SUCC_{10}$ and $PRED_1$
  - Throughput versus occupancy of the FIFO
Voltage and Delay Waveforms
Voltage and Delay Waveforms

[Graph showing voltage and time waveforms with labels:
- Dout_10
- FIRE_1
- Drift periods
- Voltage [V]
- Time [ns]

Reminder:

[Diagram showing connections:
- VDD
- VSS
- Dout_10
- FIRE_1
- SUCC_10
- PRED_1
- Long wire]
Voltage and Delay Waveforms

Reminder:

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Throughput

100% Throughput = 4.2 GDI/sec in 90nm CMOS by TSMC

Long wires impose a BIG COST on throughput
Wire Engineering

Wires are NOT FLAT – they’re TALL + SKINNY

6-4 GasP layout in 3D

- minimum width
- minimum space
- more width
- less capacitance
- more space
- less resistance
Summary

Take-Away:

• GasP will work with very long single-track wires
  • It’s CHARGE that matters, NOT TIME
  • Long wires impose a BIG COST on throughput
  • Plenty of margin to trade off length versus throughput
• True as well for ALL other single-track design

Implication:

• ENGINEER long single-track wires

PHIR MILENGE !
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AU REVOIR!