Holst Centre

Open Innovation by IMEC-NL and TNO

Extending Synchronization from Super-threshold to Sub-threshold Region

Jun Zhou, Maryam Ashouei, David Kinniment, Jos Huisken and Gordon Russell**

*IMEC Netherlands & *Newcastle University*

imec-nl

Holst Centre

Open Innovation by IMEC-NL and TNO

- Sub-threshold Operation
- Synchronization in Multi-Low-VDD Systems on Chip
- Low Voltage Synchronizer Design
- Sub-threshold Synchronizer Design
- Results
- Implementation
- Conclusion

imec-nl

Holst Centre

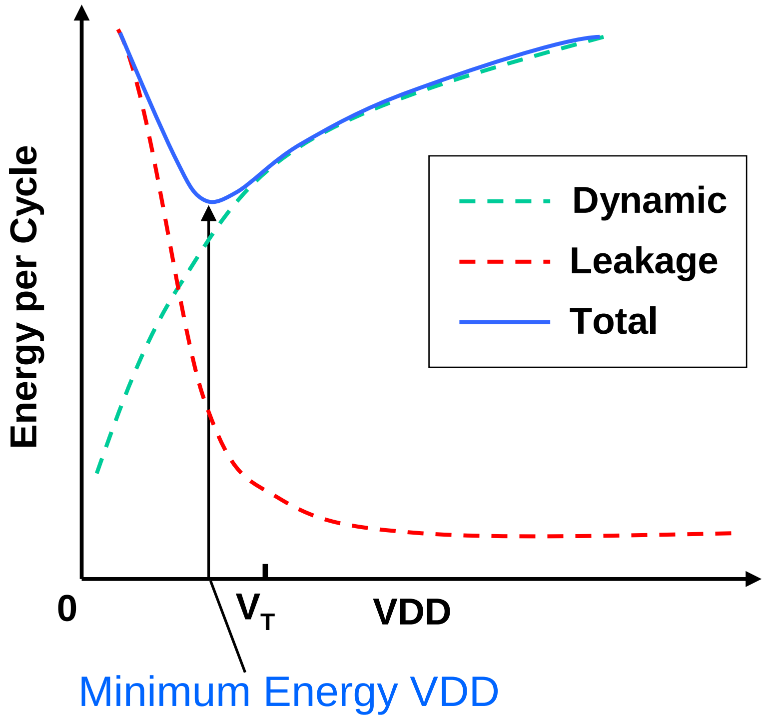
Open Innovation by IMEC-NL and TNO

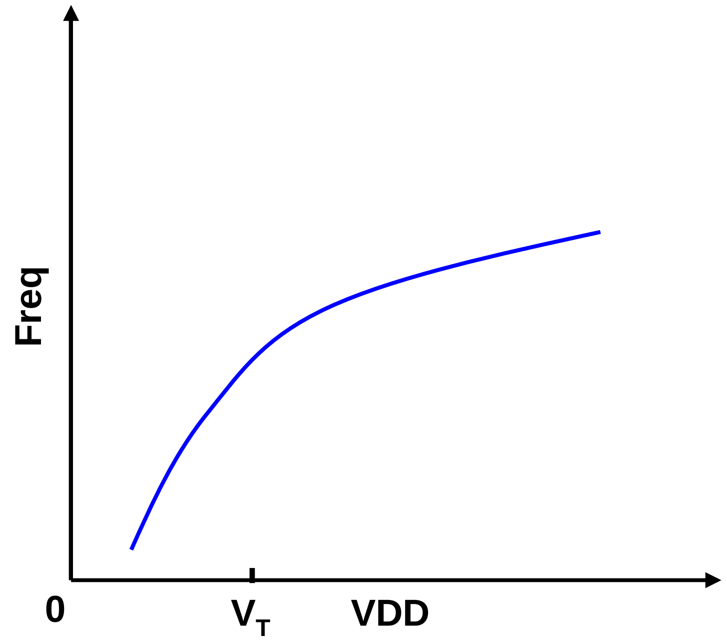
- **Sub-threshold Operation**
- Synchronization in Multi-Low-VDD Systems on Chip
- Low Voltage Synchronizer Design
- Sub-threshold Synchronizer Design
- Results
- Implementation
- Conclusion

imec-nl

Sub-threshold Operation

- **Minimum energy point VDD**
- **Low Performance Requirement**





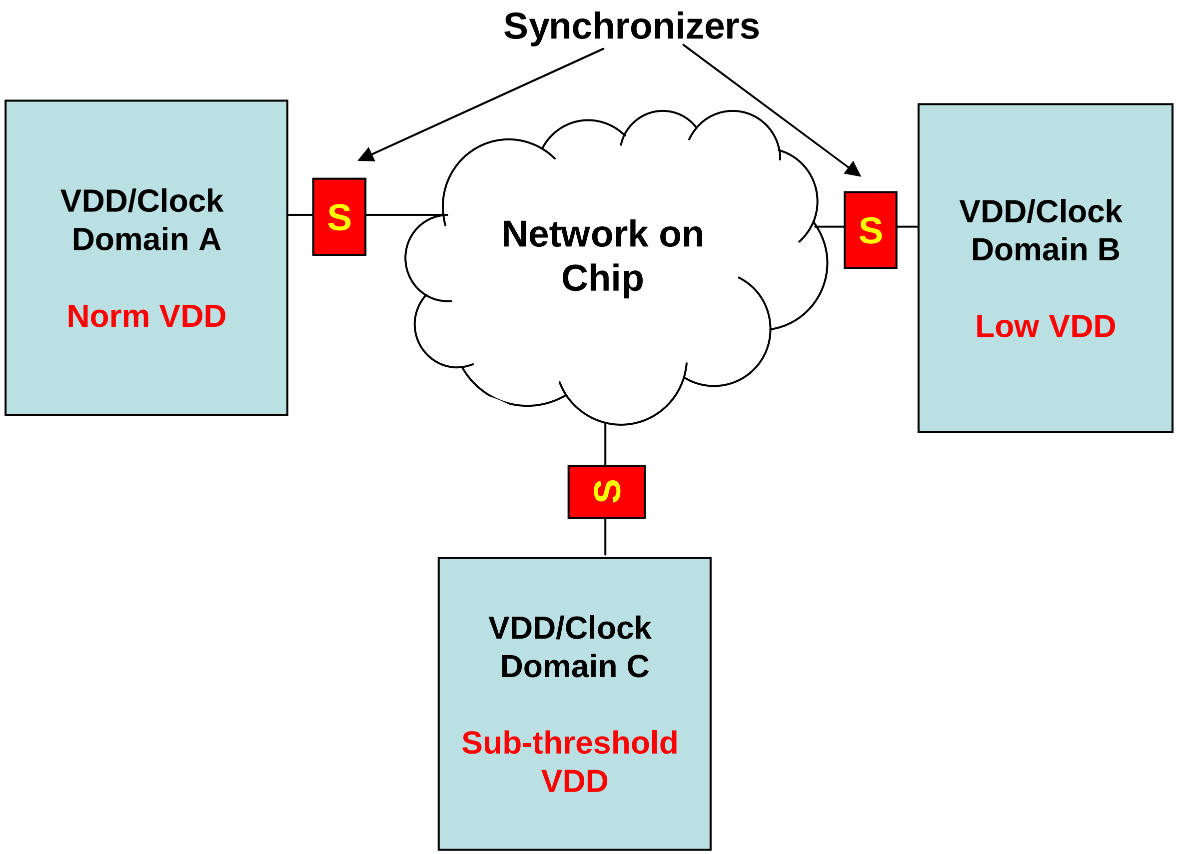
Holst Centre

Open Innovation by IMEC-NL and TNO

- Sub-threshold Operation
- **Synchronization in Multi-Low-VDD Systems on Chip**
- Low Voltage Synchronizer Design
- Sub-threshold Synchronizer Design
- Results
- Implementation
- Conclusion

imec-nl

Multi-Low-VDD Systems on Chip



Holst Centre

Open Innovation by IMEC-NL and TNO

- Sub-threshold Operation
- Synchronization in Multi-Low-VDD Systems on Chip
- **Low Voltage Synchronizer Design**
- Sub-threshold Synchronizer Design
- Results
- Implementation
- Conclusion

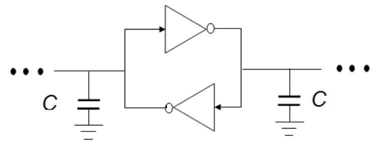
imec-nl

Synchronizer Performance (MTBF)

$$MTBF = \frac{e^{\frac{t_s - T_d}{\tau}}}{T_w f_c f_d}$$

t_s: Synchronization Time
T_d: Normal Propagation Delay
τ: Metastability Time Constant
T_w: Metastability Window
f_c: Clock Frequency
f_d: Incoming Data Frequency

In the Super-threshold Region:

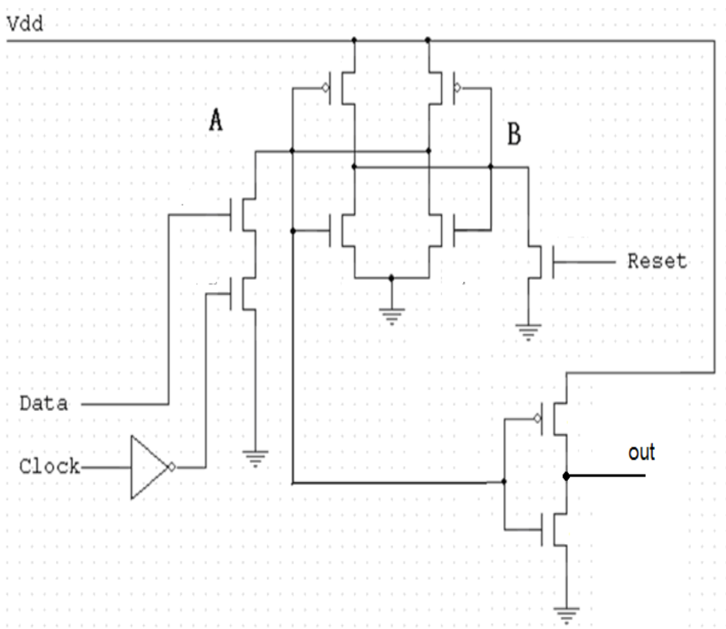


- $T_d \propto VDD, \quad VDD \downarrow \rightarrow T_d \uparrow \rightarrow MTBF \downarrow\downarrow$
- $\tau \propto \frac{C}{g_m} \quad and \quad g_m \propto I_d \propto VDD^2, \quad VDD \downarrow \rightarrow \tau \uparrow \rightarrow MTBF \downarrow\downarrow$

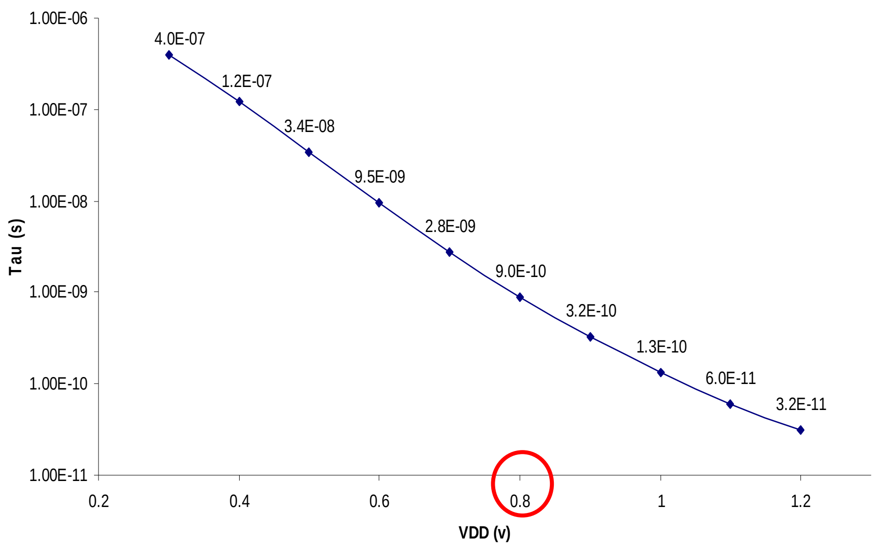
In the Sub-threshold Region:

- $T_d \propto \frac{VDD}{e^{VDD}}, \quad VDD \downarrow \rightarrow T_d \uparrow\uparrow \rightarrow MTBF \downarrow\downarrow\downarrow$
- $\tau \propto \frac{C}{g_m} \quad and \quad g_m \propto I_d \propto e^{VDD}, \quad VDD \downarrow \rightarrow \tau \uparrow\uparrow \rightarrow MTBF \downarrow\downarrow\downarrow$

Jamb Latch

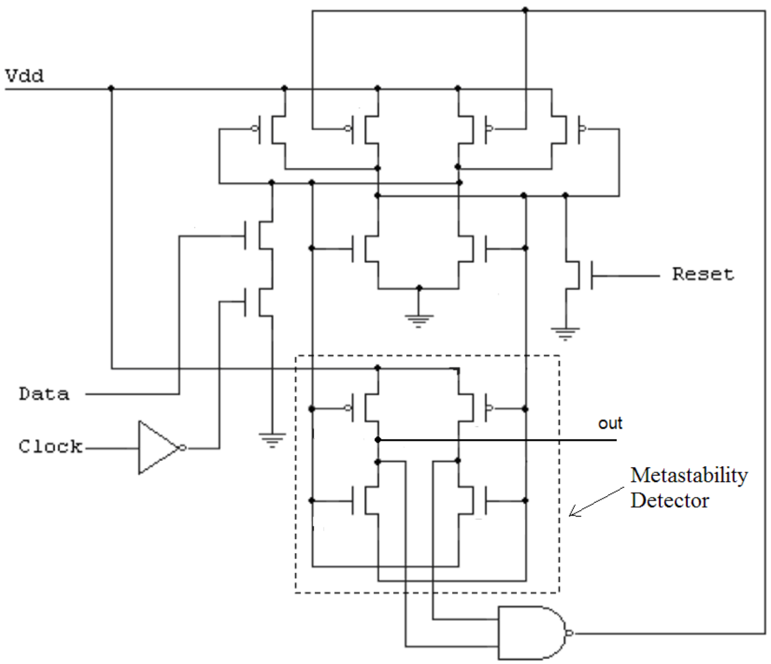


Schematic

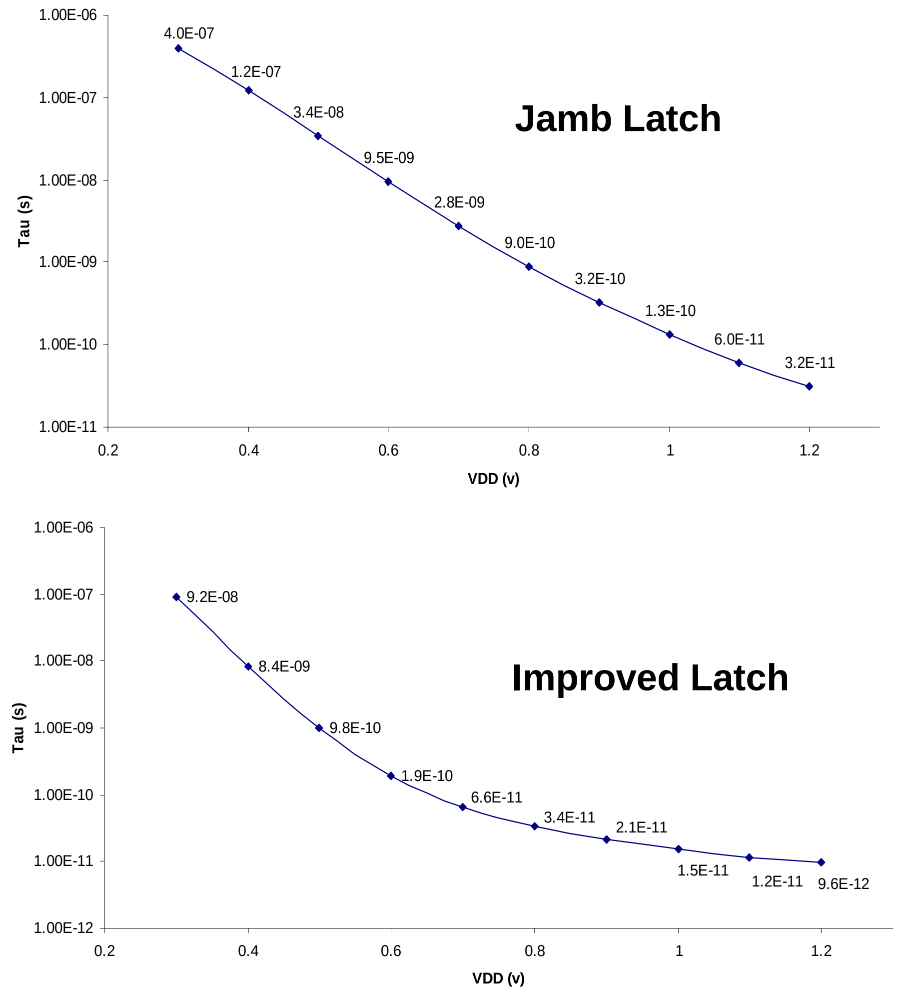


τ vs VDD

Improved Latch

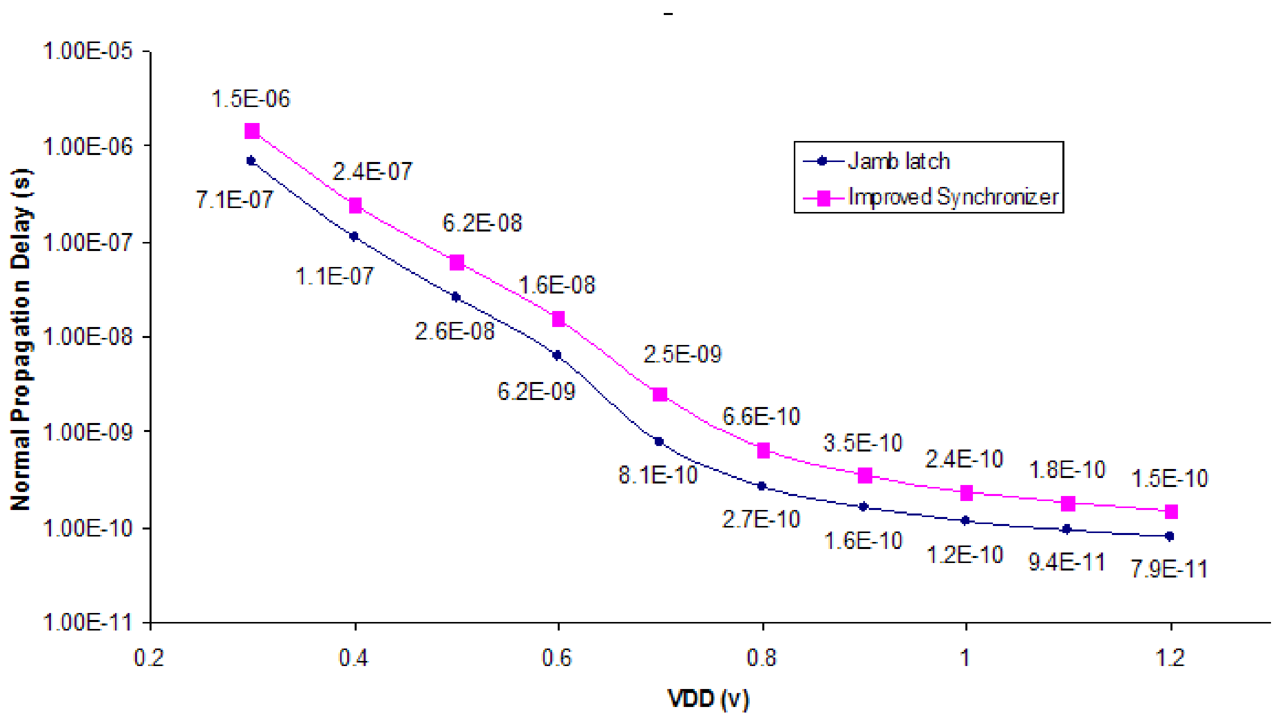


Schematic



τ vs VDD

Normal Propagation Delay T_d



Sub-threshold MTBF

$$MTBF = \frac{e^{\frac{t_s - T_d}{\tau}}}{T_w f_c f_d}$$

At 0.3 V, T_w = 30 ~ 50 ns. Assuming that $f_c = f_d$ = 300 KHz:

	τ	T_d	*MTBF*
Jamb Latch	400 ns	0.7 us	0.17 s
Improved latch	92 ns	1.5 us	2 days

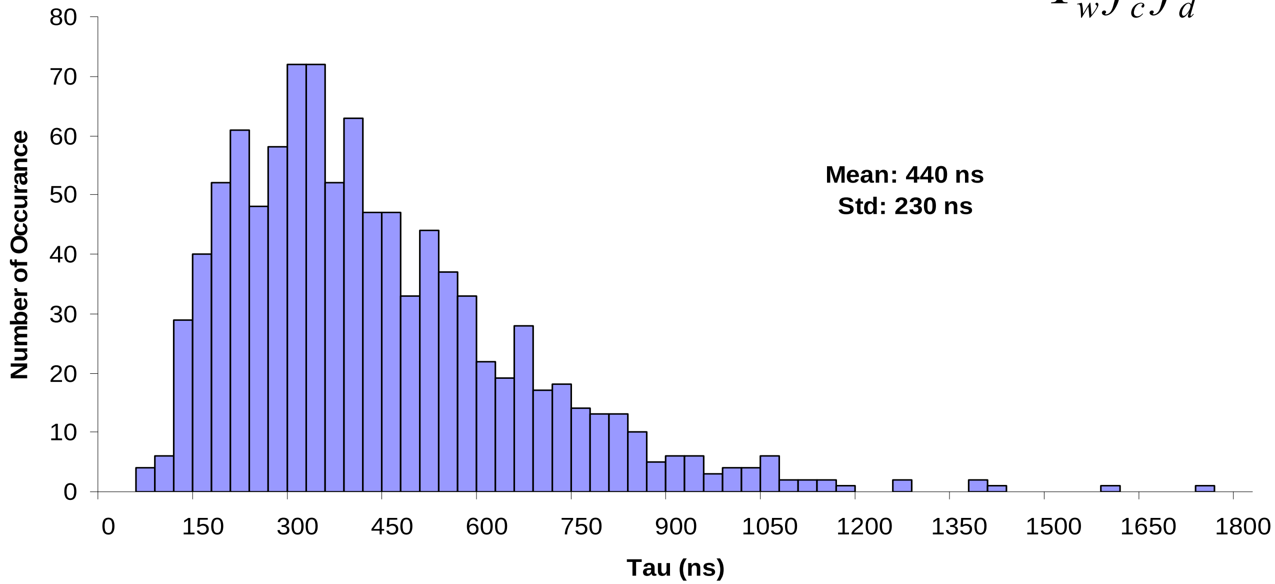
Unacceptable !

Two factors are not taken into account in the calculation:

1. System MTBF = Single MTBF / Num of Synchronizers
2. Large Process Variation in the Sub-Threshold Region

Process Variation

$$MTBF = \frac{e^{\frac{t_s - T_d}{\tau}}}{T_w f_c f_d}$$



Variation of Tau for Jamb Latch at 0.3 V

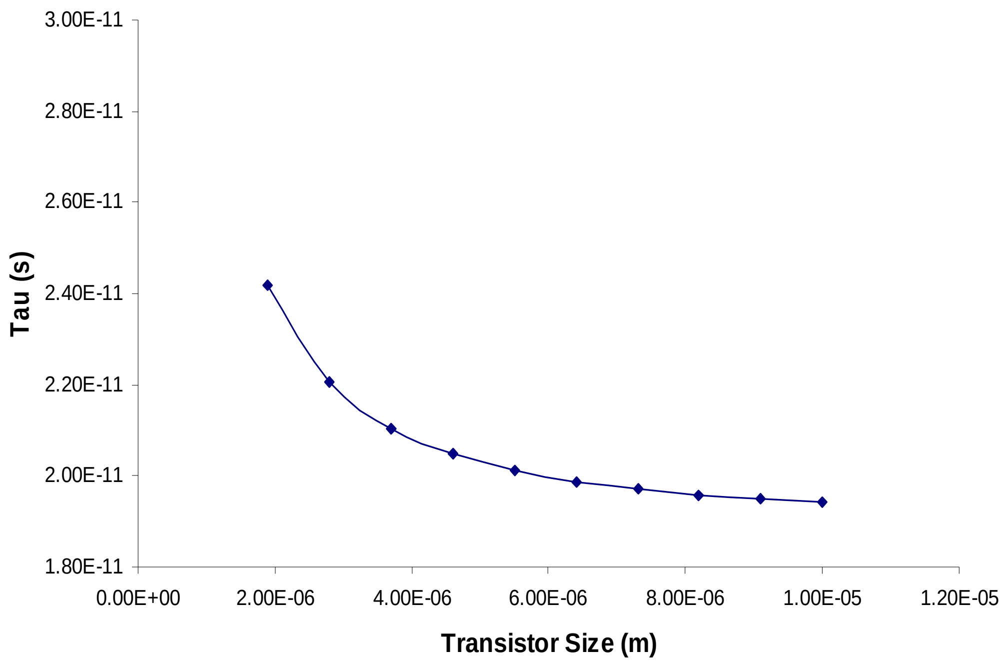
Holst Centre

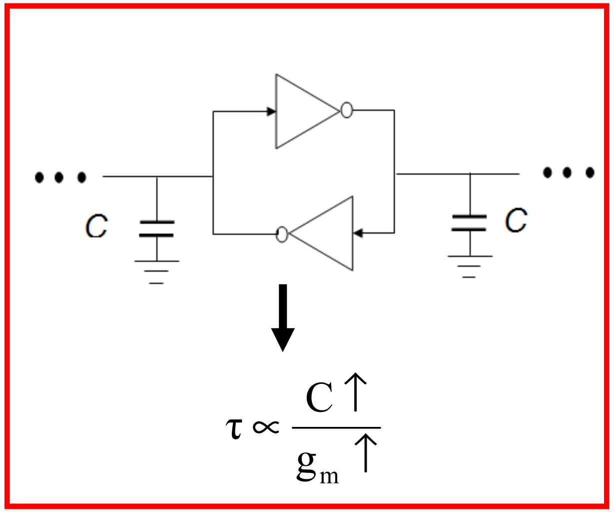
Open Innovation by IMEC-NL and TNO

- Sub-threshold Operation
- Synchronization in Multi-Low-VDD Systems on Chip
- Low Voltage Synchronizer Design
- **Sub-threshold Synchronizer Design**
- Results
- Implementation
- Conclusion

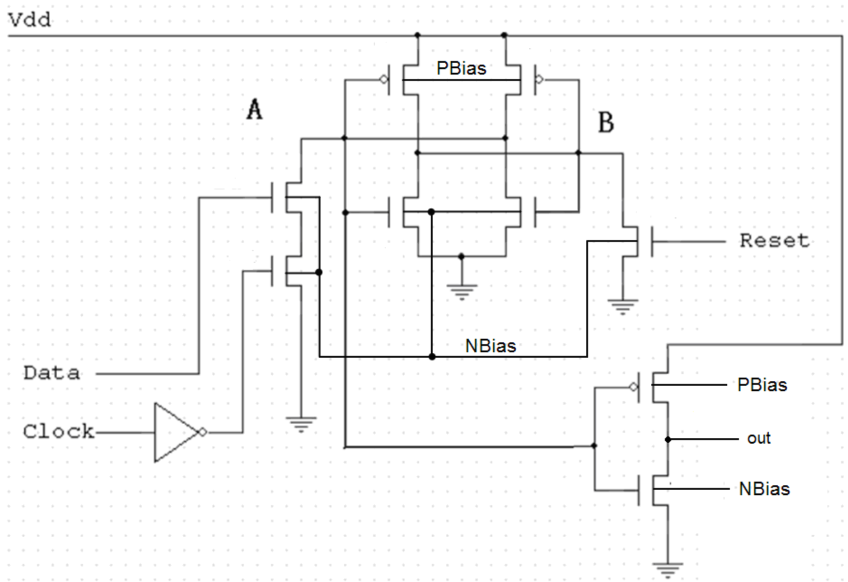
imec-nl

Increasing Transistor Size?





Applying Forward Body Bias (FBB)



Advantages:

1. **Increase g_m without increasing C. So tau is reduced.**
2. **Propagation delay is reduced like other logic circuits.**
3. **Process variation is improved.**

Super-threshold: $g_m = \mu_n \cdot C_{ox} \frac{W}{L} \cdot (V_{gs} - V_T)$

Sub-threshold: $g_m = \frac{I_d}{n \cdot v_{th}}, \quad I_d \propto e^{-V_T}$

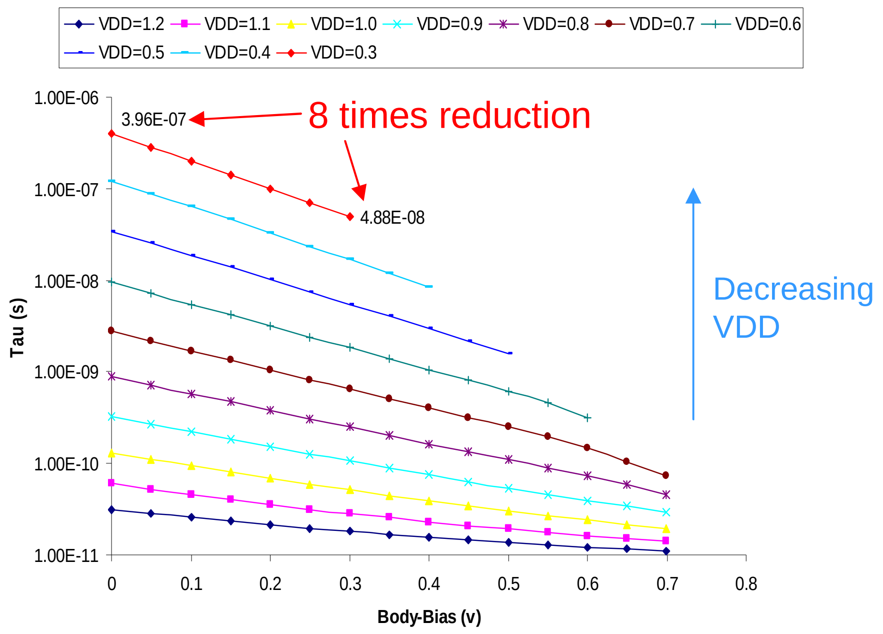
Holst Centre

Open Innovation by IMEC-NL and TNO

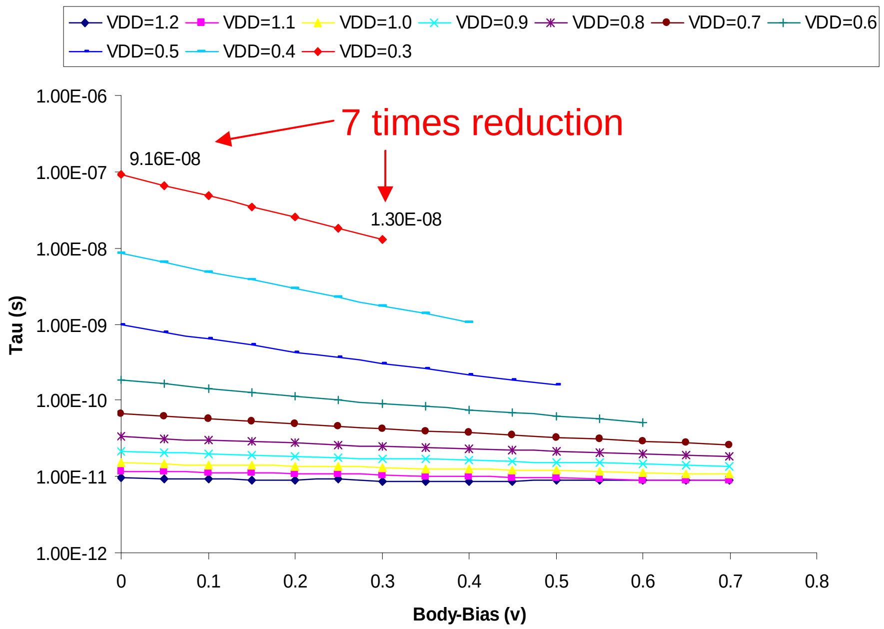
- Sub-threshold Operation
- Synchronization in Multi-Low-VDD Systems on Chip
- Low Voltage Synchronizer Design
- Sub-threshold Synchronizer Design
- **Results**
- Implementation
- Conclusion

imec-nl

Tau vs FBB

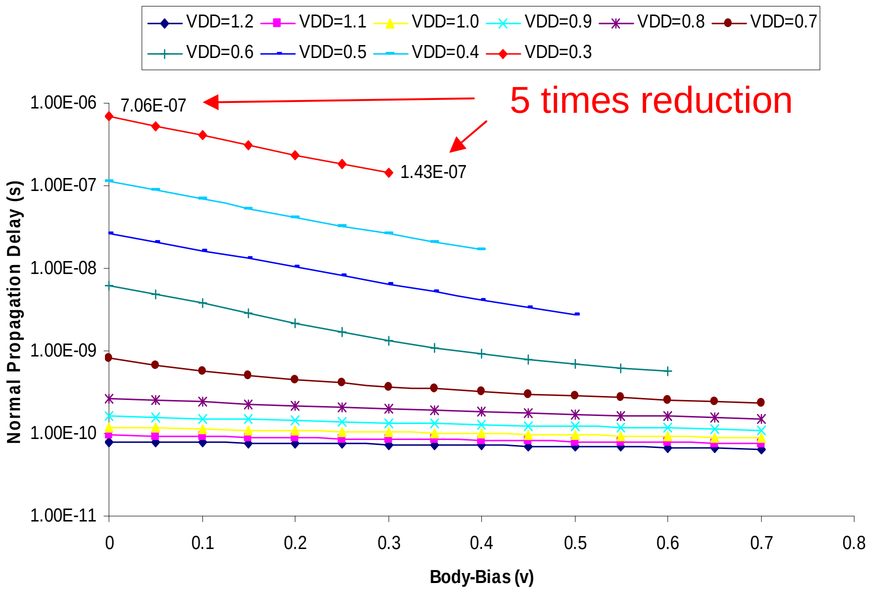


Jamb Latch with FBB

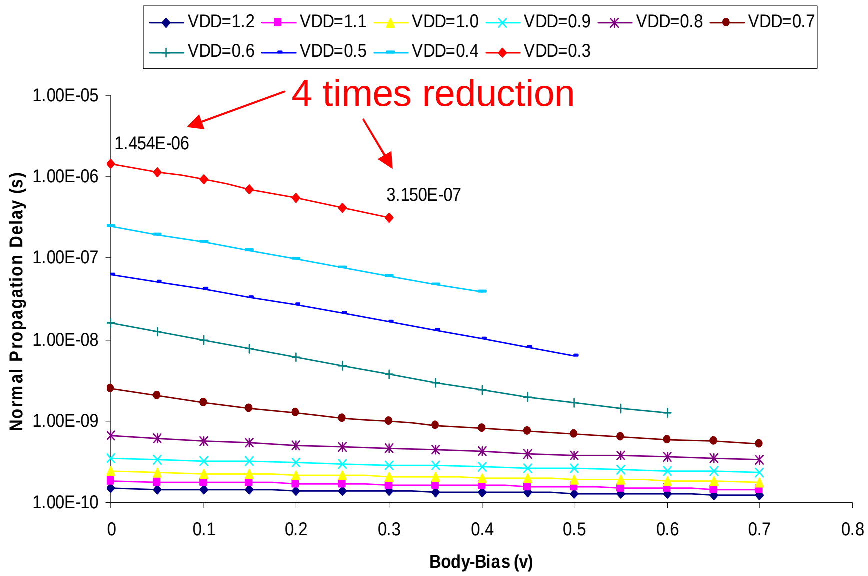


Improved Latch with FBB

Propagation Delay vs FBB

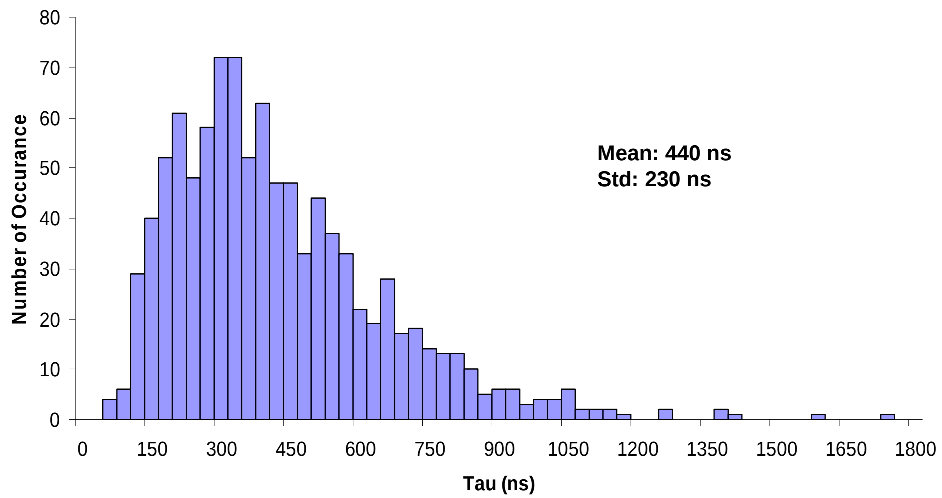


Jamb Latch with FBB

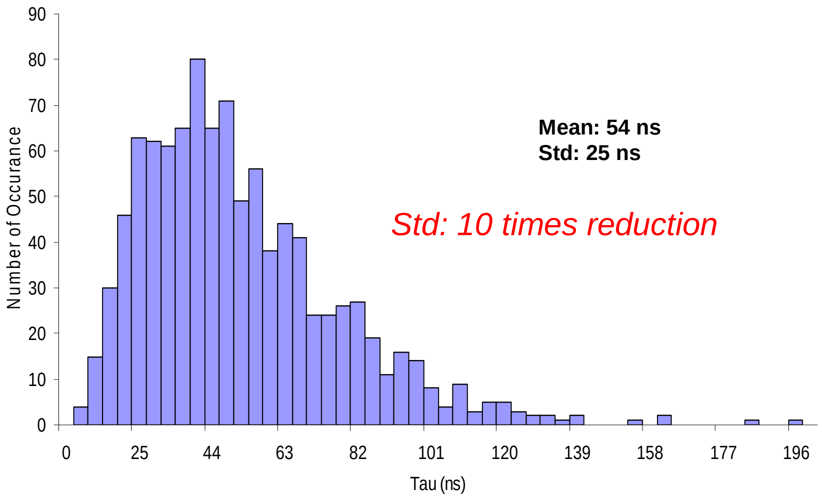


Improved Latch with FBB

Process Variation



Without FBB at 0.3 V



With FBB at 0.3 V

Sub-threshold MTBF

$$MTBF = \frac{e^{\frac{t_s - T_d}{\tau}}}{T_w f_c f_d}$$

At 0.3 V, Tw = 7 ~ 15 ns, assuming that $f_c = f_d$ = 300 KHz:

	τ	T_d	*MTBF*
Jamb Latch	400 ns	0.7 us	0.17 s
Improved latch	92 ns	1.5 us	2 days
Jamb Latch with 0.3V FBB	49 ns	0.14 us	1.35×10^{17} years
Improved Latch with 0.3V FBB	13 ns	0.32 us	4.88×10^{89} years

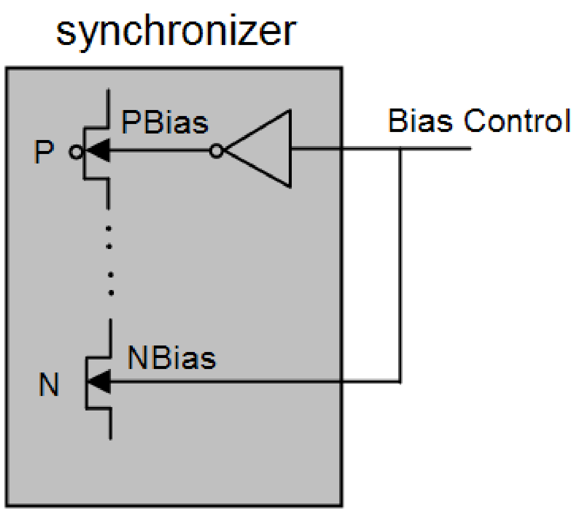
3σ → 4.7 months

Holst Centre

Open Innovation by IMEC-NL and TNO

imec-nl

Full-VDD Biased Synchronizer



Advantage:

1. *Full-VDD bias gives large performance improvement.*

2. *No on-chip voltage generation circuit needed (Min Power and Area Overhead).*

3. *The Bias can be disabled when VDD is higher than the PN junction conducting voltage (0.7 V) to avoid performance degradation.*

Holst Centre

Open Innovation by IMEC-NL and TNO

- Sub-threshold Operation
- Synchronization in Multi-Low-VDD Systems on Chip
- Low Voltage Synchronizer Design
- Sub-threshold Synchronizer Design
- Results
- Implementation
- **Conclusion**

imec-nl

Conclusions

1. For the first time, synchronizer performance is investigated in the near-threshold and sub-threshold region.
2. The investigated synchronizers shows unacceptable MTBF especially when taking into account the process variation.
3. Applying Forward Body Bias significantly improves Td and Tau. It also greatly reduce the impact of process variation on synchronizer performance. As a result, MTBF is significantly improved.
4. A full-VDD biased synchronizer scheme is proposed to improve synchronizer performance in the near-threshold and sub-threshold region with minimal area and power overhead.

Thank you !

Question?