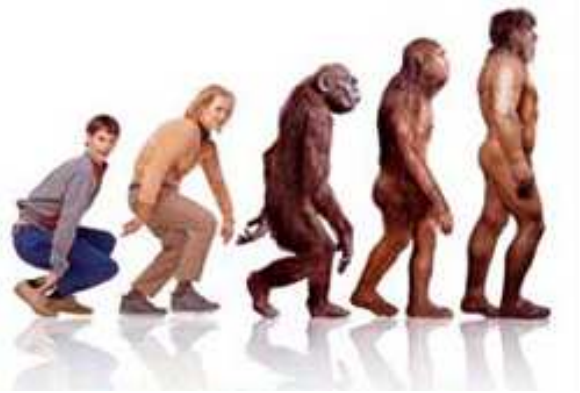
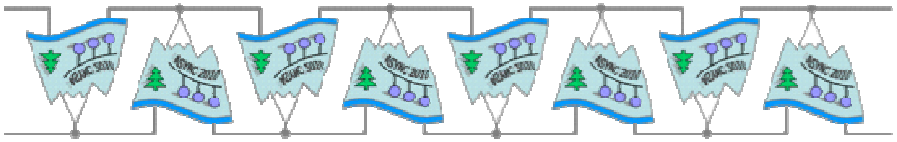
The Devolution of Synchronizers

Salomon Beer,**
*Ran Ginosar**
*Michael Priel***
*Rostislav (Reuven) Dobkin**
*Avinoam Kolodny**



*Electrical Engineering Dept, Technion—Israel Institute of Technology
**Freescale Semiconductor

Technion Israel Institute of Technology



freescale semiconductor

Outline

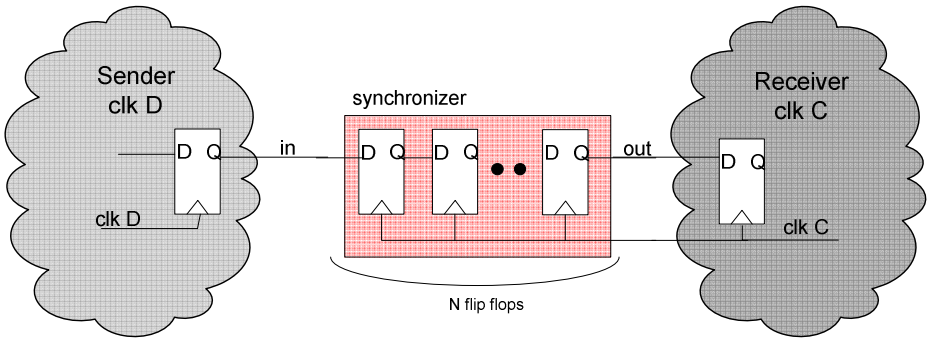
- **Introduction**
- First signs of devolution
  - SoC measurements
- Further Confirmation of devolution
  - FPGA measurements
- How can we explain devolution
  - Model
- Implications & Conclusions

Synchronizers

- Simple failure rate model of latches and FF

$$MTBF = \frac{e^{S/\tau}}{T_W \times F_C \times F_D}$$

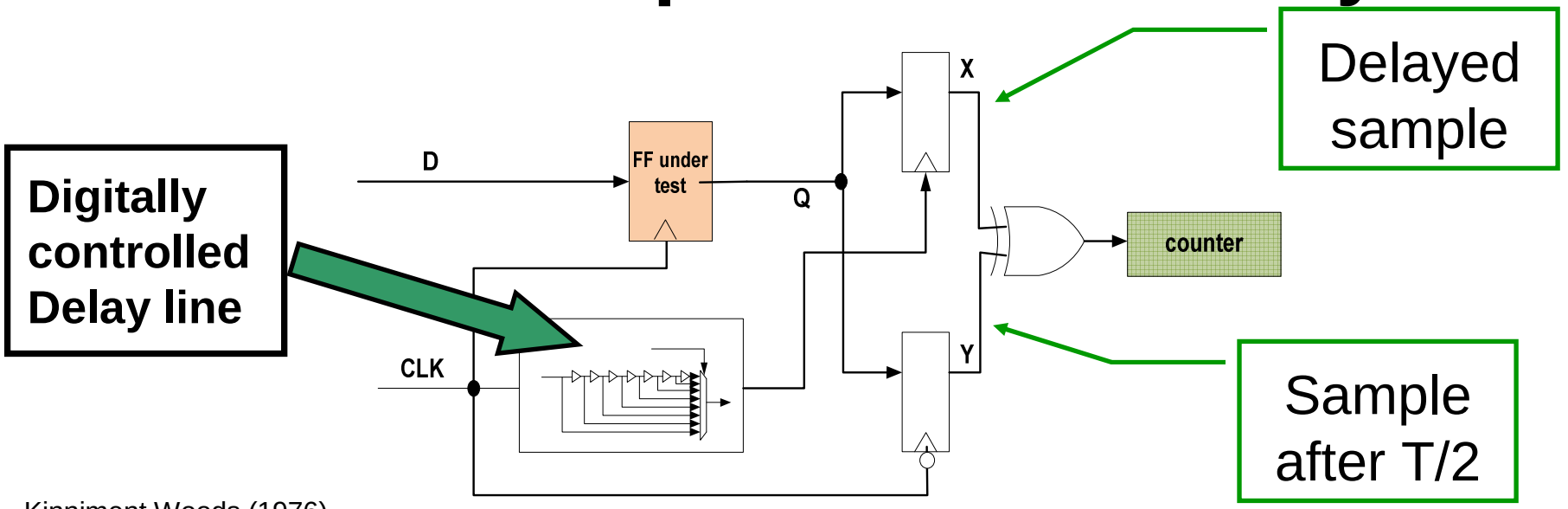
- Synchronizer performance figure of merit (τ *dominant*)
  - Fast recovery (low τ)→ Good synch.
  - Slow recovery (high τ) → Bad synch
- τ was believed to scale down with technology
- Rule of thumb to design "reliable" synch was : $\tau \approx 2 \cdot FO4$



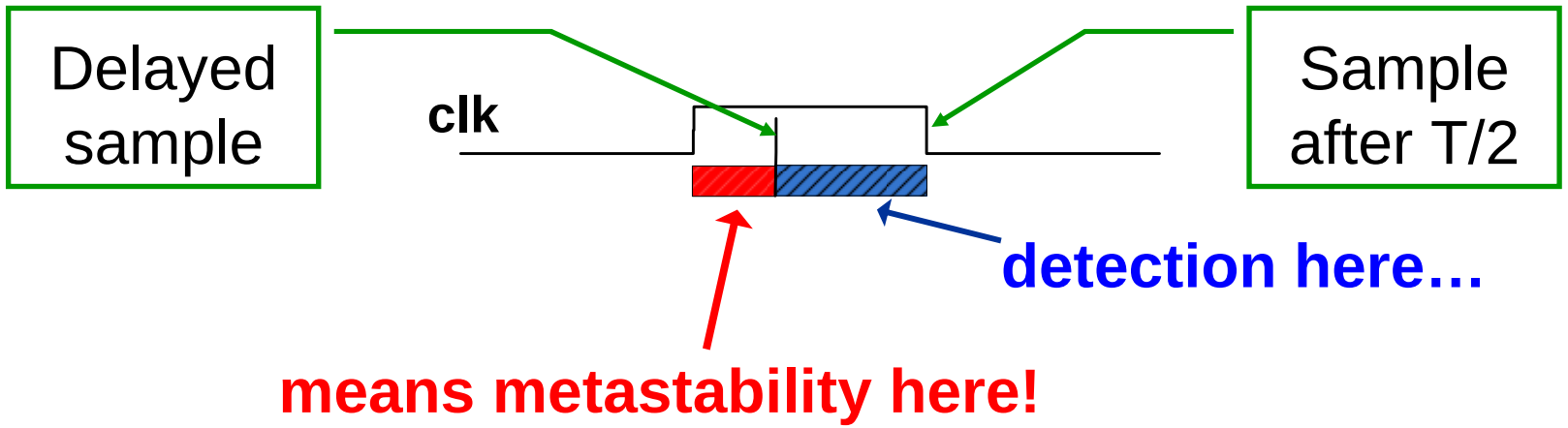
Outline

- Introduction
- **First signs of devolution**
  - **SoC measurements**
- Further Confirmation of devolution
  - FPGA measurements
- How can we explain devolution
  - Model
- Implications & Conclusions

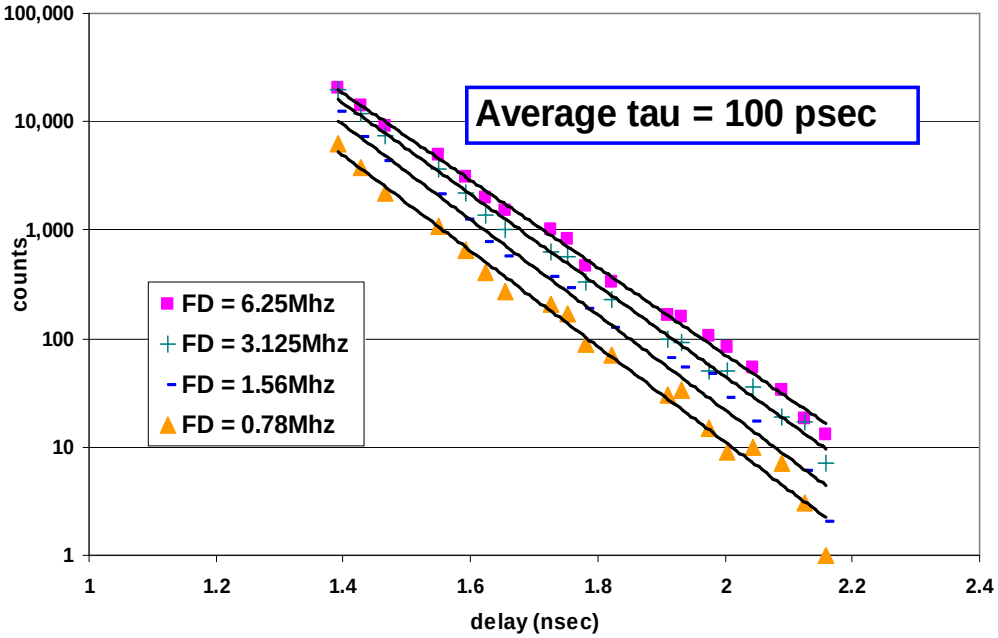
On-chip measurement system

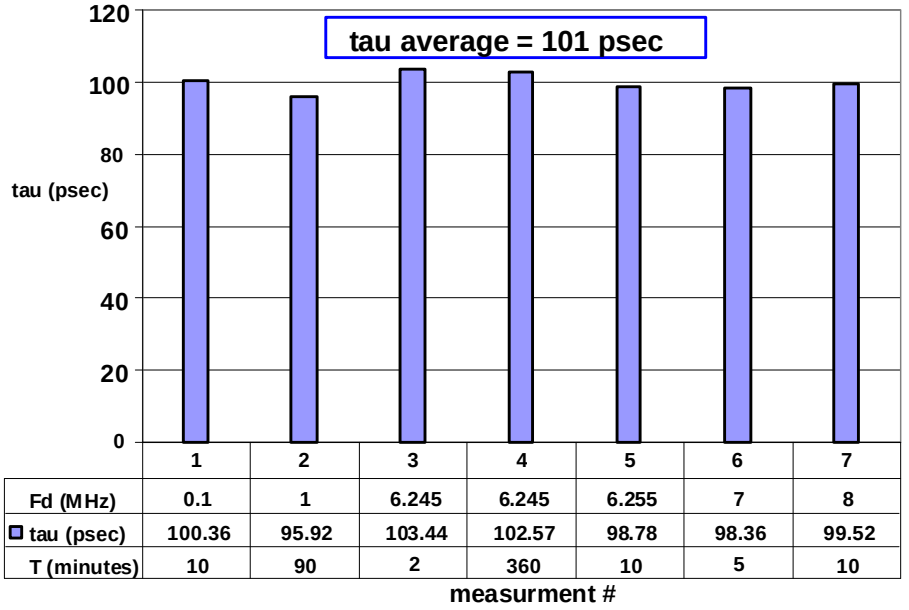


Kinniment Woods (1976)



Measurement Results





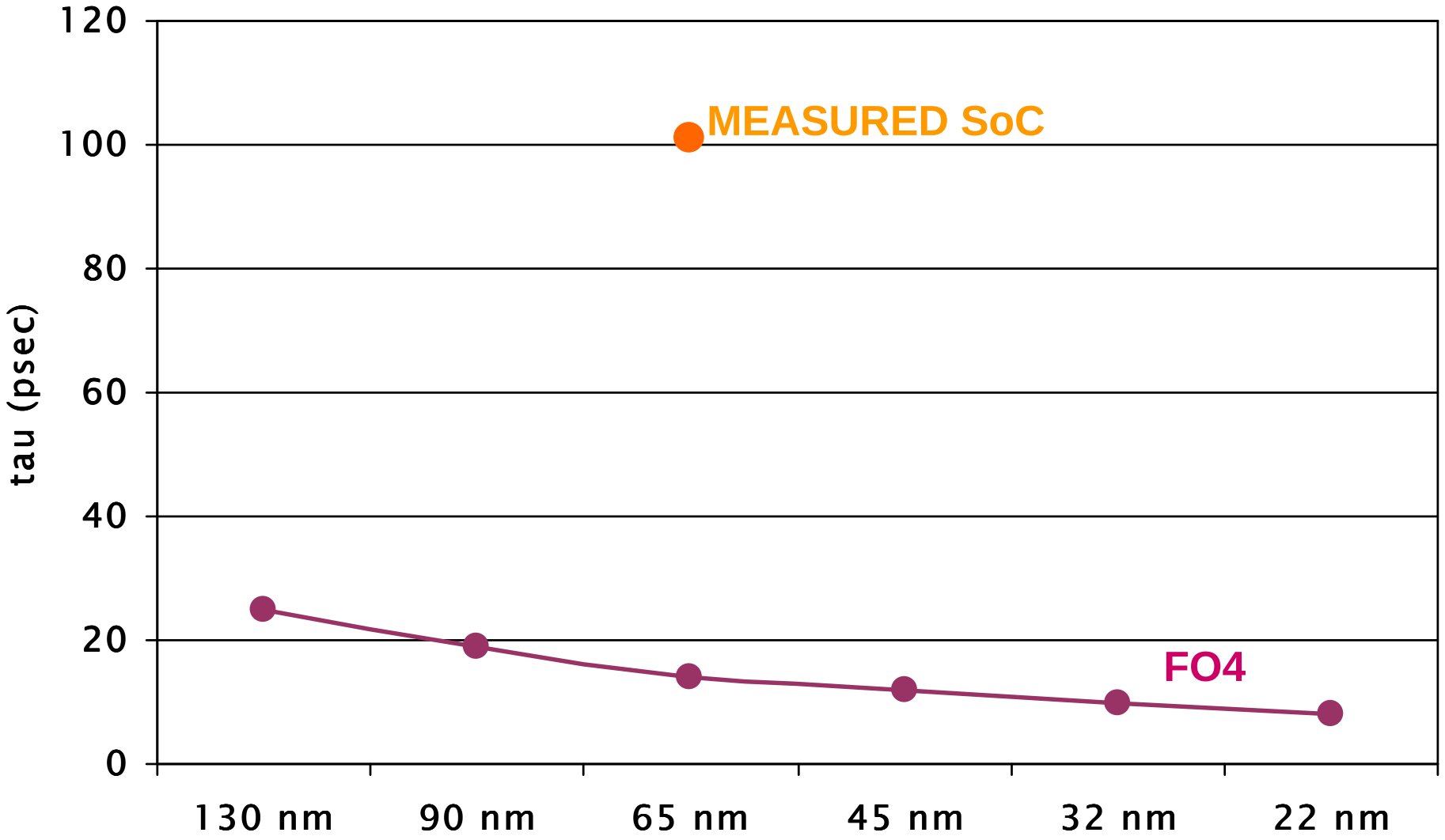
	1	2	3	4	5	6	7
Fd (MHz)	0.1	1	6.245	6.245	6.255	7	8
tau (psec)	100.36	95.92	103.44	102.57	98.78	98.36	99.52
T (minutes)	10	90	2	360	10	5	10

tau values higher than expected

First signs of devolution

- A 65nm bulk CMOS TC fabricated
- τ for several FF measured using on-chip measurement system.
- Measured: τ *~100 psec*
- Expected: τ ~ *56psec*
  - *FO4 of LP 65nm ~ 28 psec*

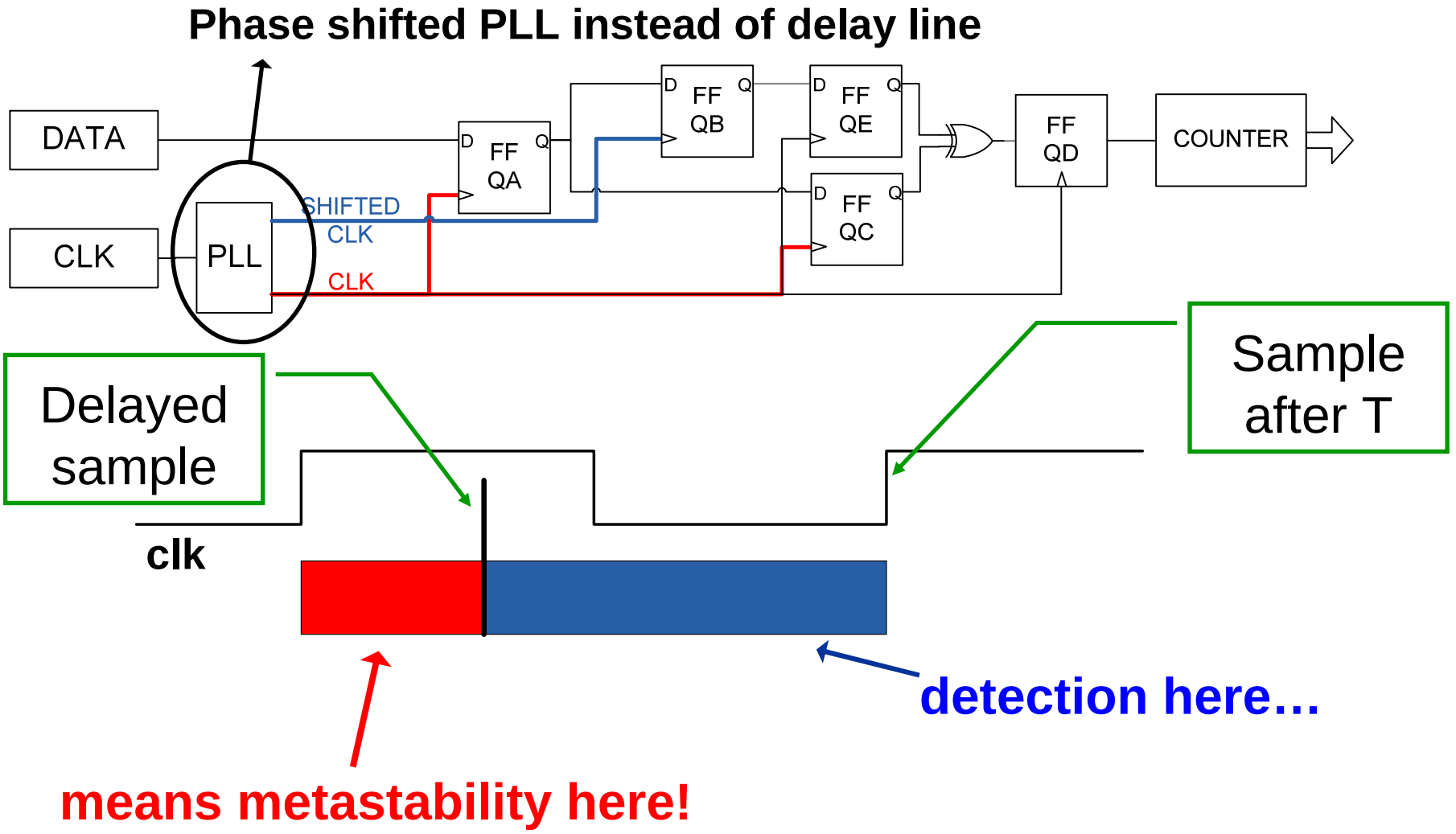
Unified graph of τ trend



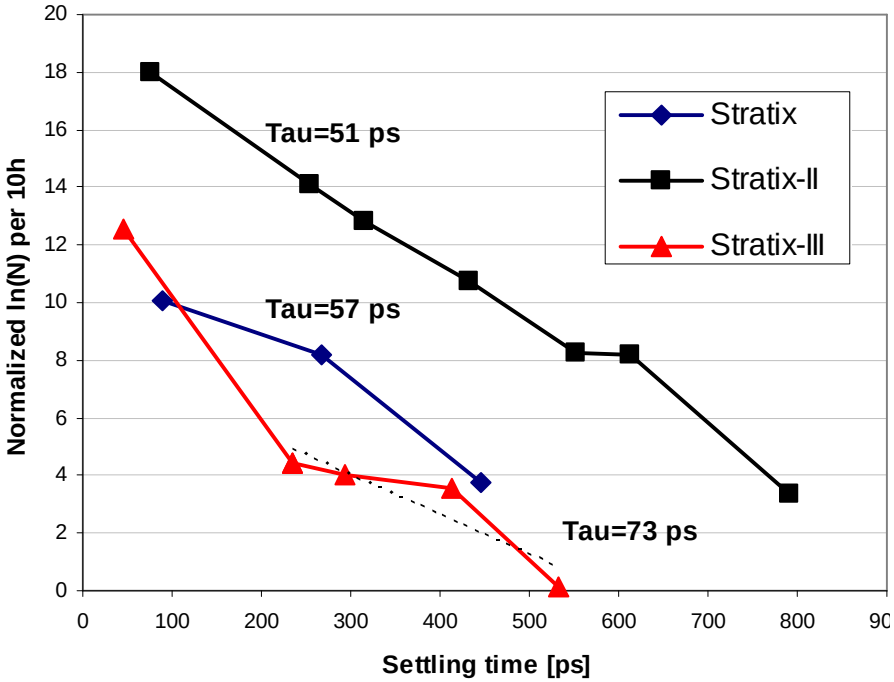
Outline

- Introduction
- First signs of devolution
  - SoC measurements
- Further Confirmation of devolution
  - FPGA measurements
- How can we explain devolution
  - Model
- Implications & Conclusions

Measurement method

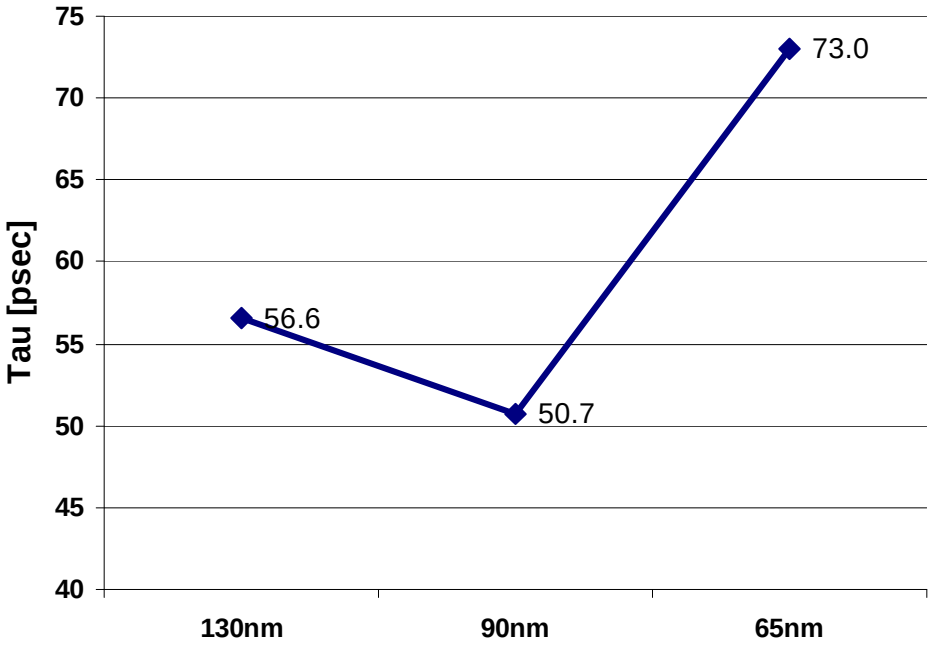


Altera FPGA results



exponential behavior

scaling degradation

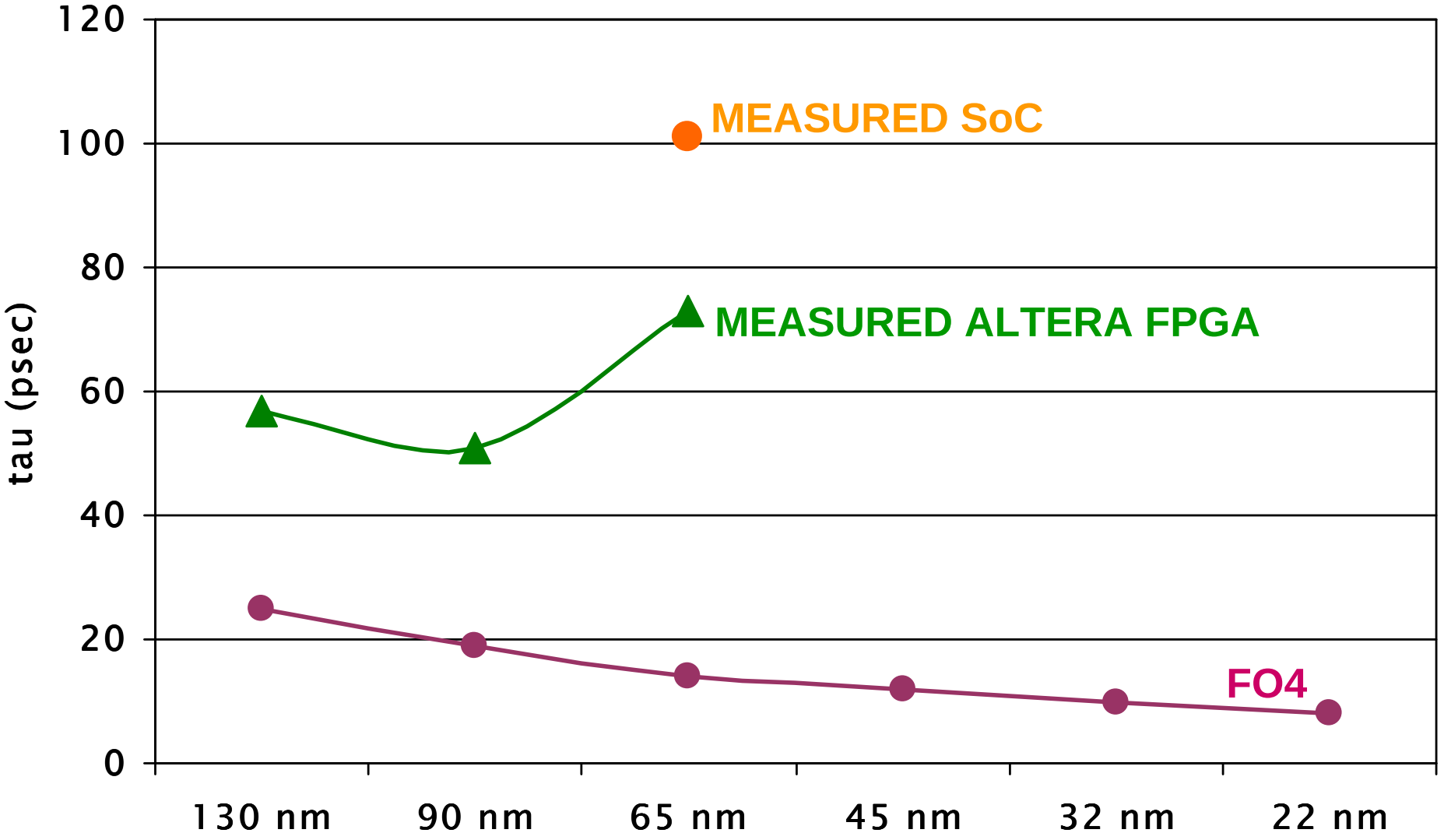


Altera FPGA Measurements

- Three generations of similar FPGA devices measured:
  - Stratix (130 nm)
  - Stratix II (90 nm)
  - Stratix III (65 nm)

- Internal LAB/CLB FF was used as synchronizer
- Measuring method similar to SoC, under FPGA constraints
- Internal delay compensated

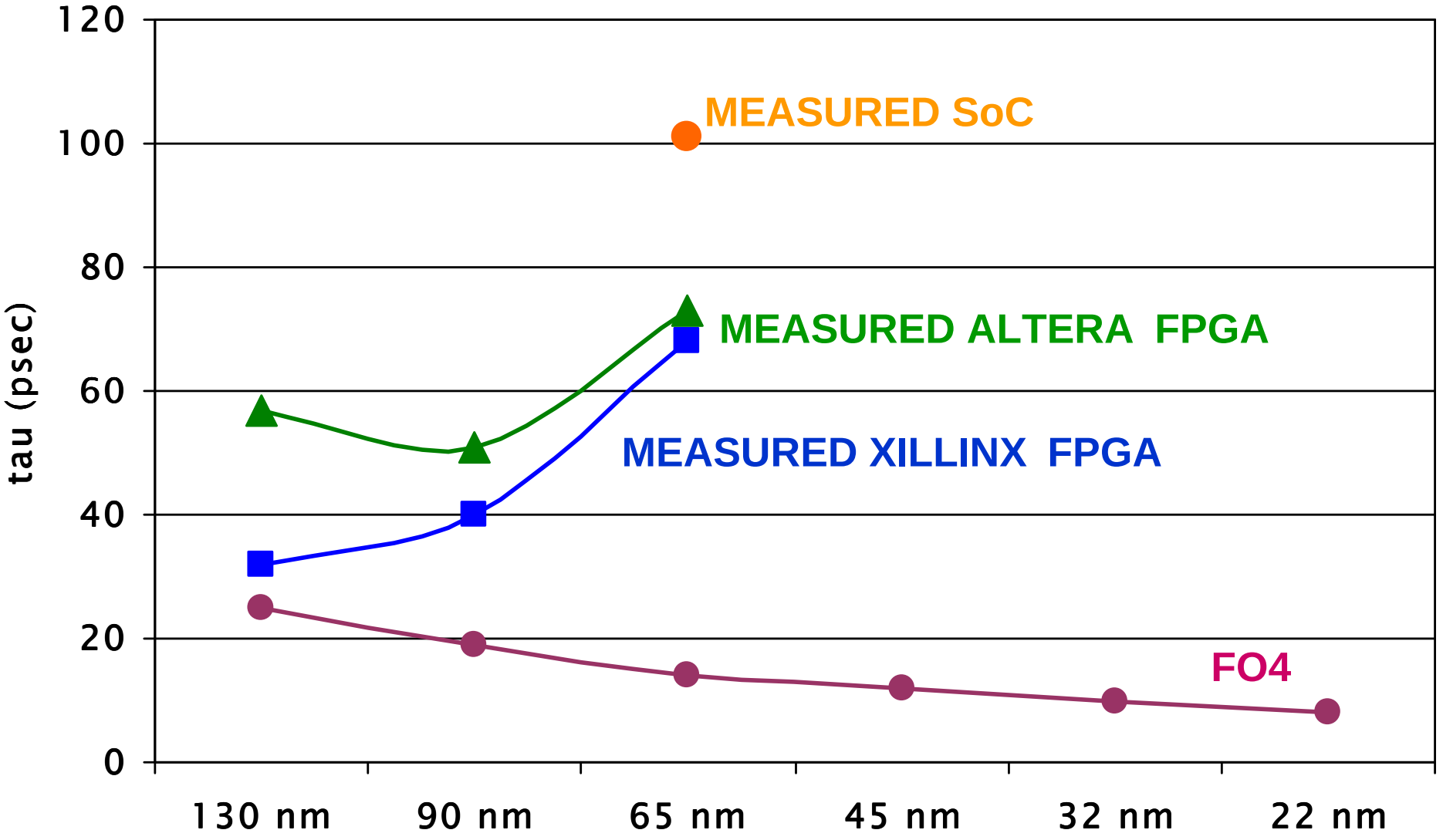
Unified graph of τ trend



Xilinx FPGA Measurements

- P. Alfke measured 3 generations of devices:
  - Virtex II-pro (130 nm)
  - Virtex 4 (90 nm)
  - Virtex 5 (65 nm)
- Internal FPGA FF were measured
- Different measuring method
  - Varying frequency instead of delay

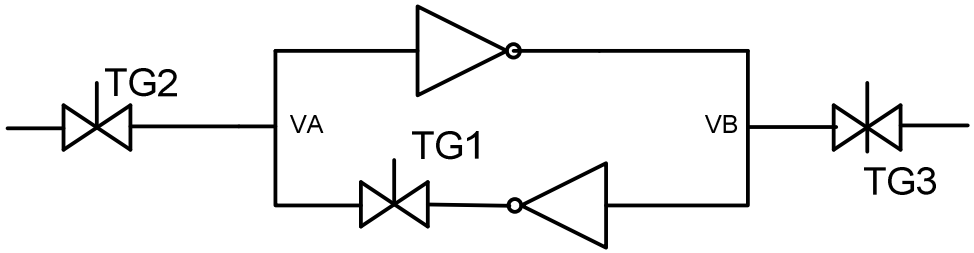
Unified graph of τ trend

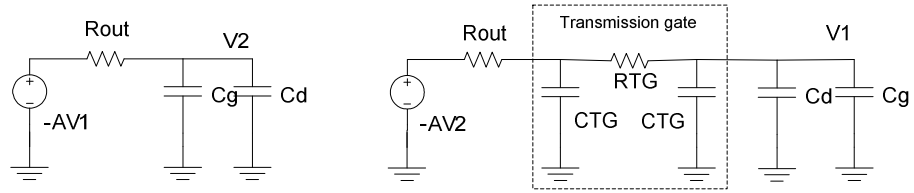


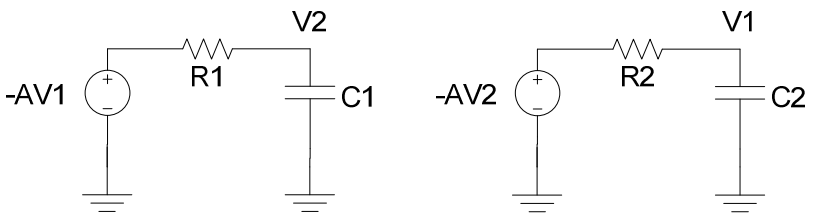
Outline

- Introduction
- First signs of devolution
  - SoC measurements
- Further Confirmation of devolution
  - FPGA measurements
- **How can we explain devolution**
  - **Model**
- Implications & Conclusions

Latch Model







$$\tau = \frac{\eta}{4}\frac{FO4}{A}$$

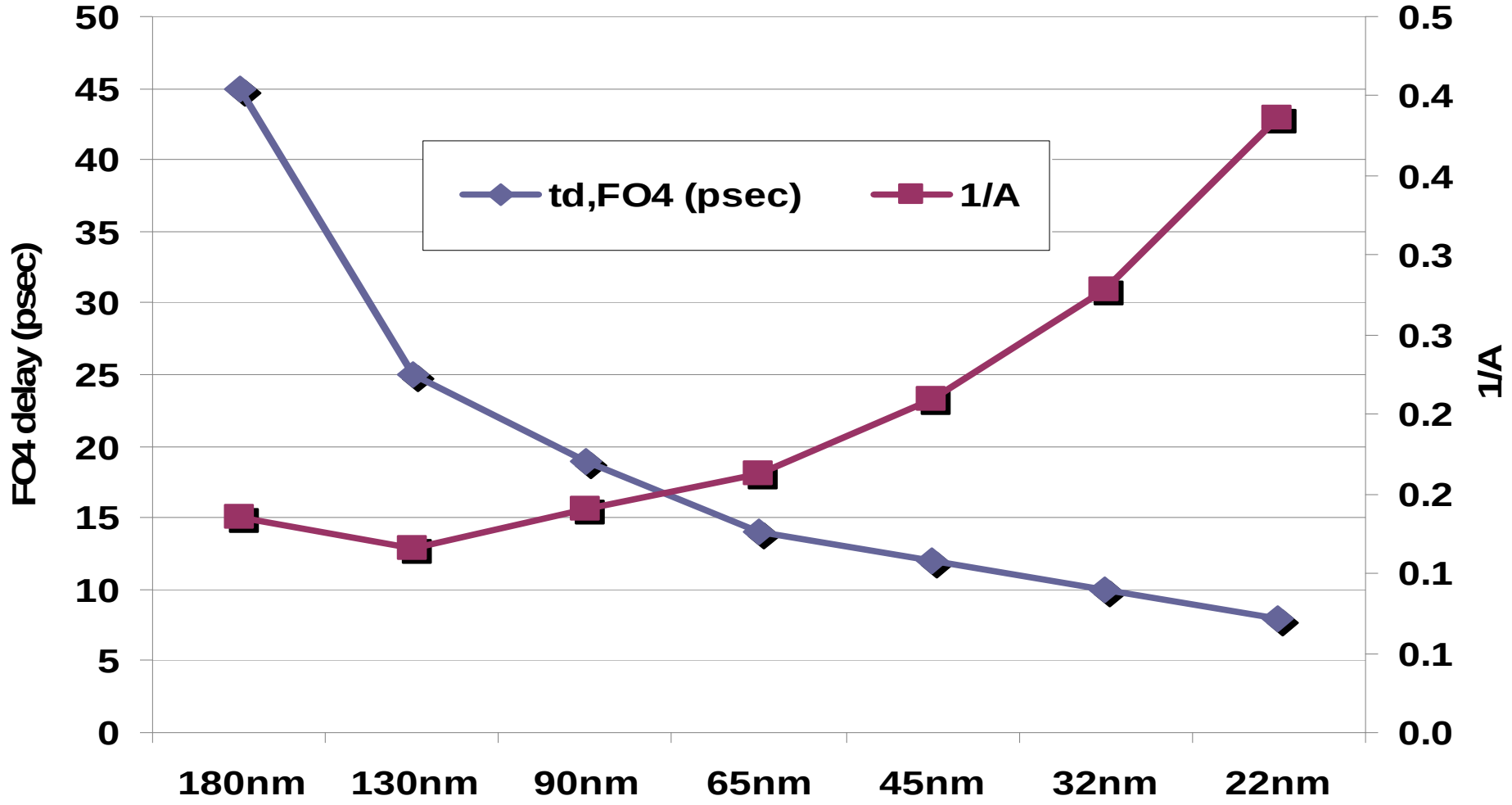
$$\eta \approx \frac{2}{3}\frac{1}{\lambda \cdot V_{DD}}\left(\frac{V_{DD} - V_T}{\frac{V_{DD}}{2} - V_T}\right)$$

λ **Channel length modulation (CLM)**

Two new factors, η and A

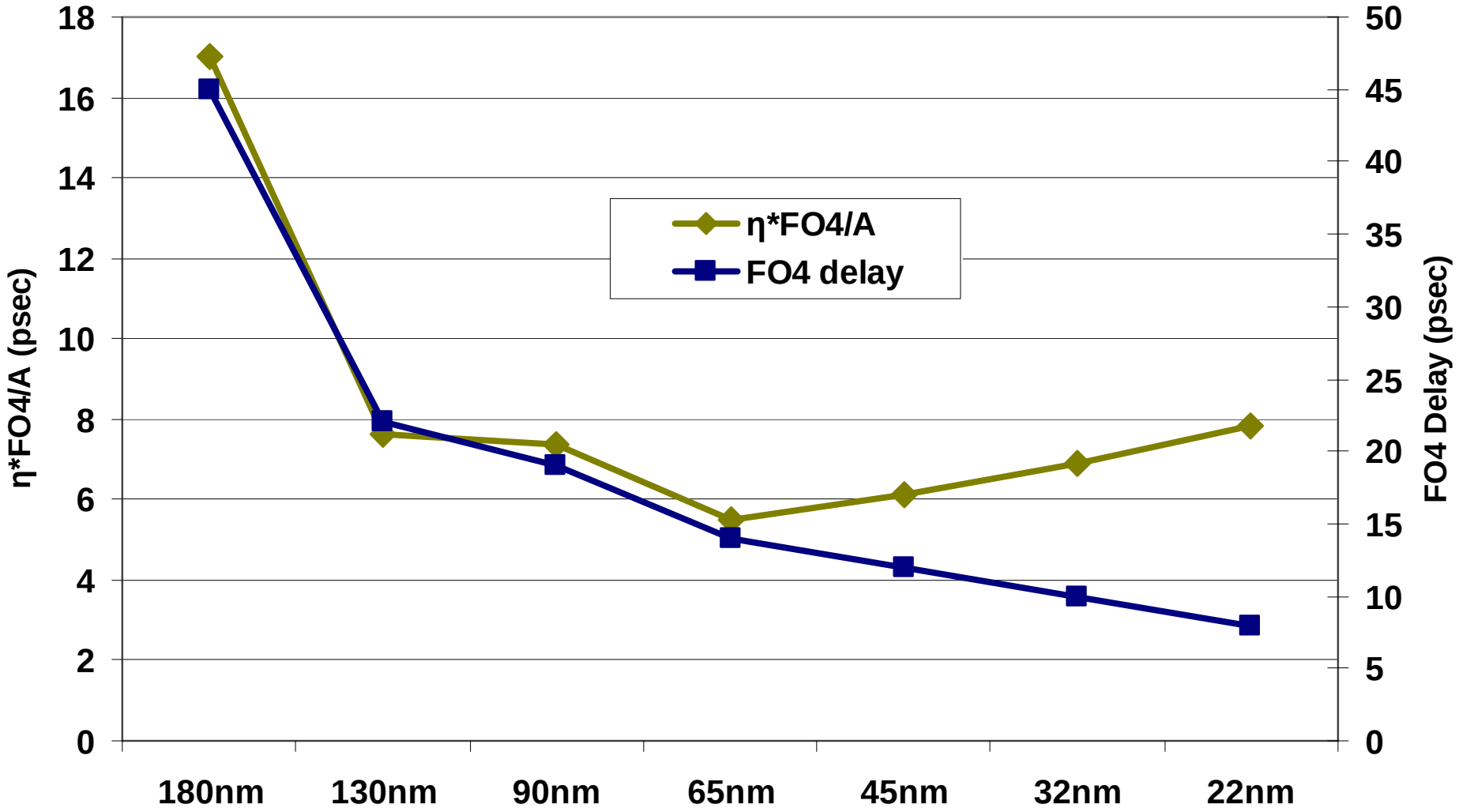
$$\tau = \frac{\eta}{4}\frac{FO4}{A}$$

Delay vs Gain tradeoff



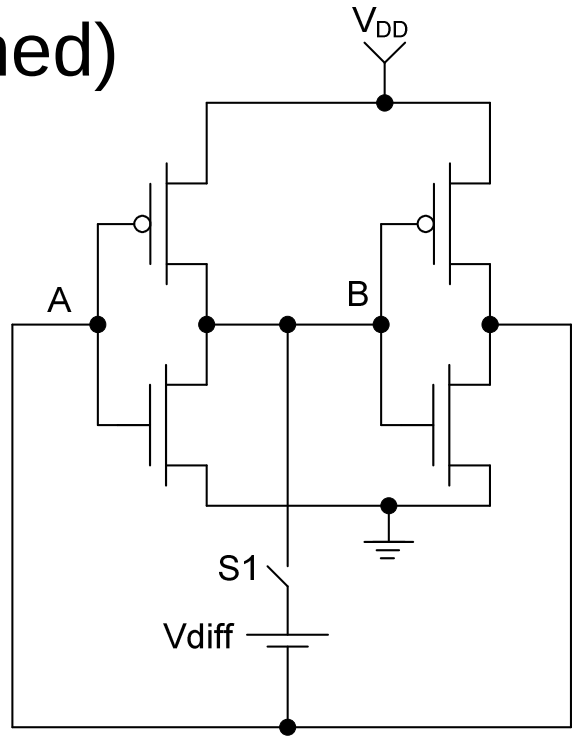
$$\tau = \frac{\eta}{4}\frac{FO4}{A}$$

Simulating η, A



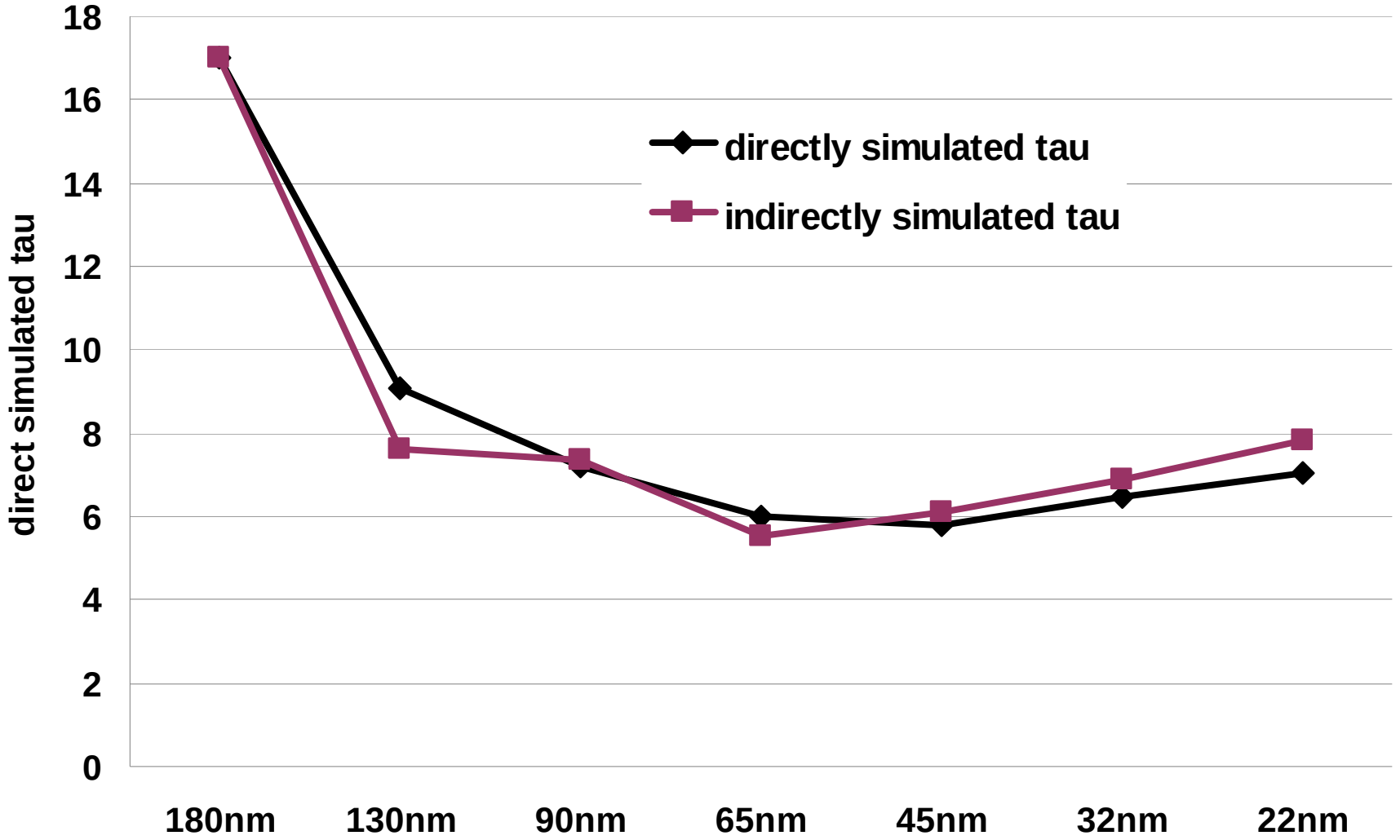
Direct simulations

- Latch is forced into metastability
  - S1 closed
- Switch (S1) is then released (opened)
- Latch resolves

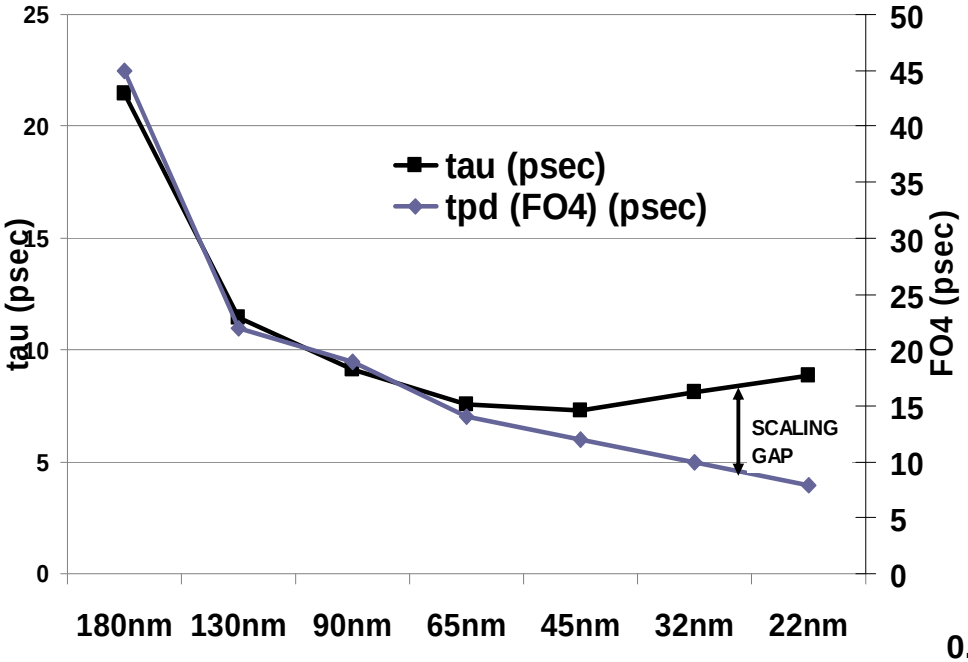


Dike and Burton (1999)

Direct and Indirect simulations

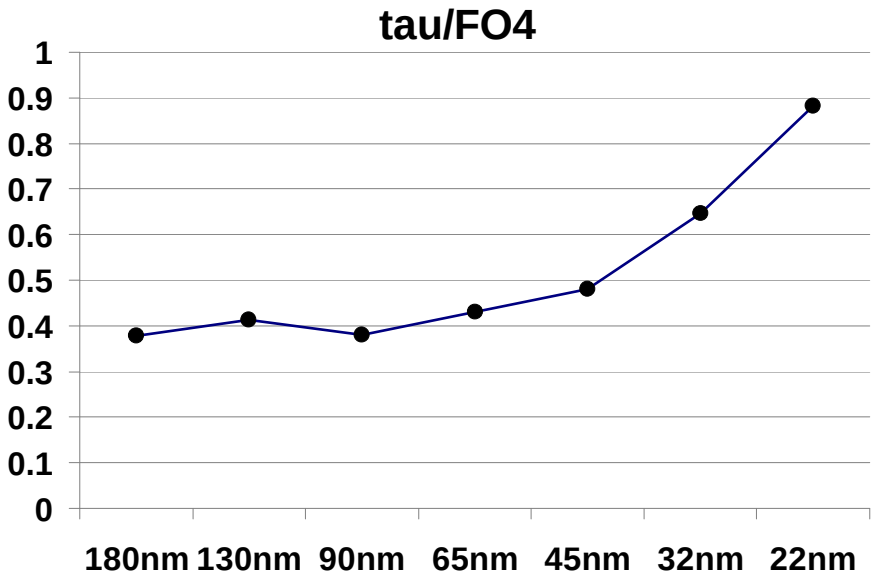


Simulation results

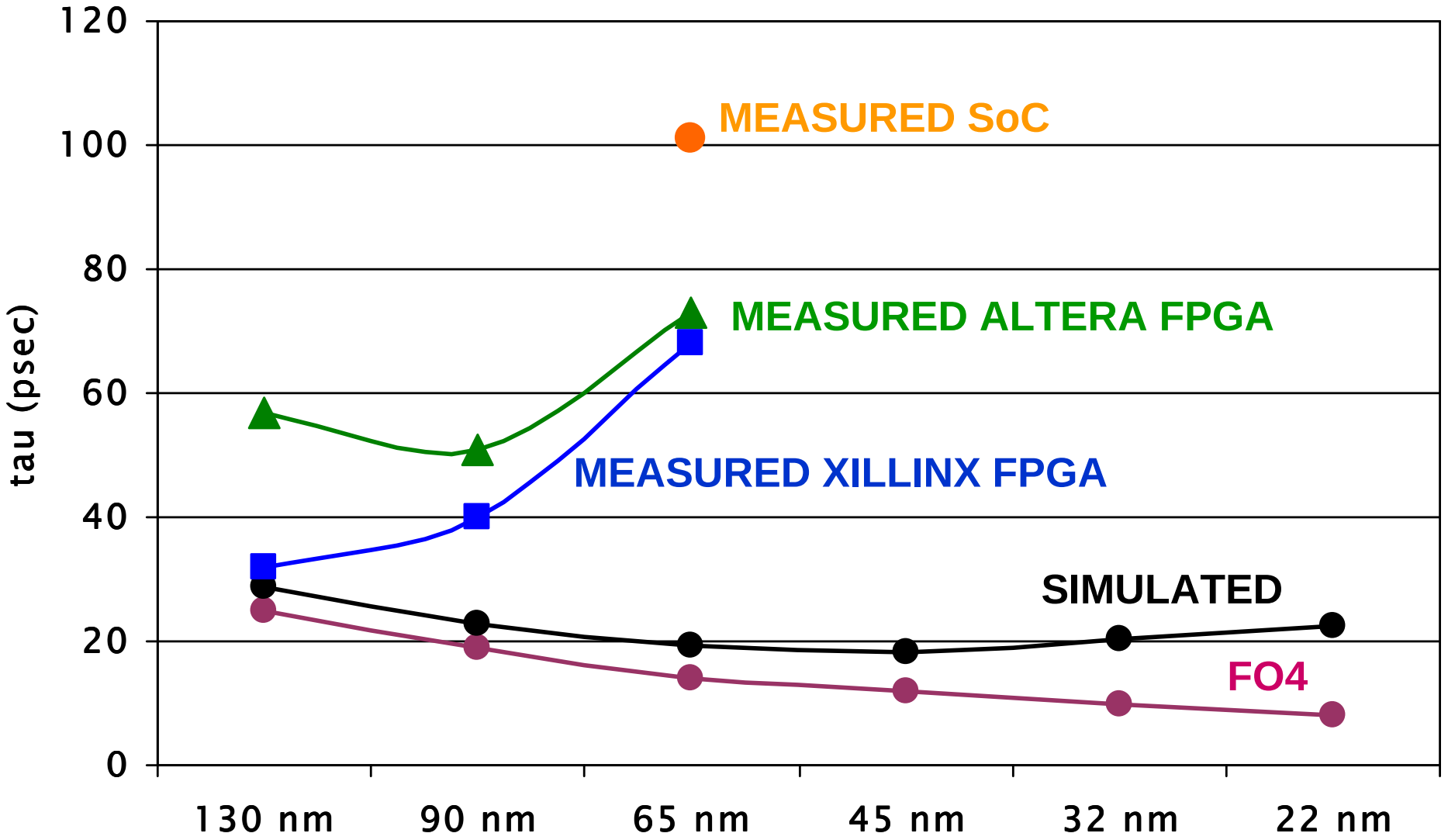


scaling GAP

$$\kappa = \frac{\tau}{FO4}$$



Unified graph of τ trend



Outline

- Introduction
- First signs of devolution
  - SoC measurements
- Further Confirmation of devolution
  - FPGA measurements
- How can we explain devolution
  - Devolution model
- **Implications & Conclusions**

?=

Remarks

- τ decreases until an inflection point and then increases with scaling.
- Inflection point:
  - Predicted :45nm node
  - Measured :65nm node

  } Optimistic model
- Different circuit design of FF → trend
- Process flavors (GP, LP, HVT, LVT, etc.) affect τ
  - LP → high FO4 → high τ
  - GP → low FO4 → low τ
- Process Variations

New rule of thumb

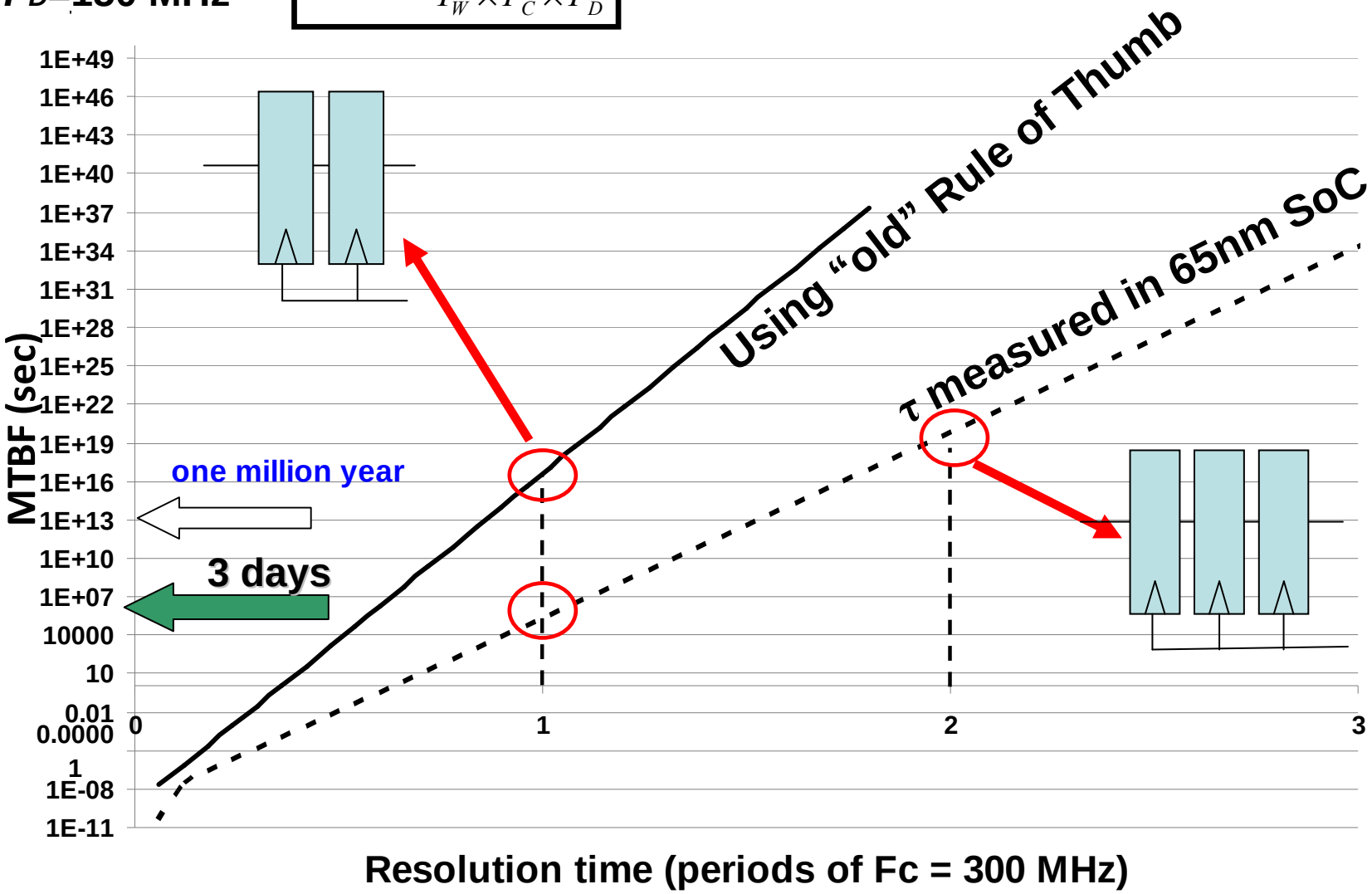
- No Rule of Thumb
- $\tau = \kappa \cdot FO4$,K=2 was good till 65nm tech.
- Future technologies will need characterization and adapted value of K.

Reliability example

F_C=300 MHz

F_D=150 MHz

$$MTBF = \frac{e^{S/\tau}}{T_W \times F_C \times F_D}$$



Conclusions

- τ increases with scaling
  - *τ degradation effect*
- Three parameter Model

$$\tau = \frac{\eta}{4}\frac{FO4}{A}$$

- Simple rule of thumb fails
  - Don’t re-use blindly
- *Characterize each process*

Questions