

A 128 x 128 x 24Gb/s Crossbar,  
Interconnecting 128 tiles in a single hop,  
and Occupying 6% of their area

Giorgos Passas, Manolis Katevenis, Dionisis Pnevmatikatos

presentation by  
Giorgos Passas

Inst. of Computer Science (ICS)  
Foundation for Research & Technology -- Hellas (FORTH)  
Heraklion, Crete, Greece

## - Goal

- Through real ASIC design
- Area cost estimation of high-valency crossbar datapaths

## - Contribution

- ASIC design of a 128x128x24Gbps crossbar NoC, which occupies less than 6% of a typical die

## - Applications

- CMPs
  - a crossbar NoC with above 100 ports
- Combined input-output queued switch chips
  - speeding up a high-valency switch with 10Gb/s IO

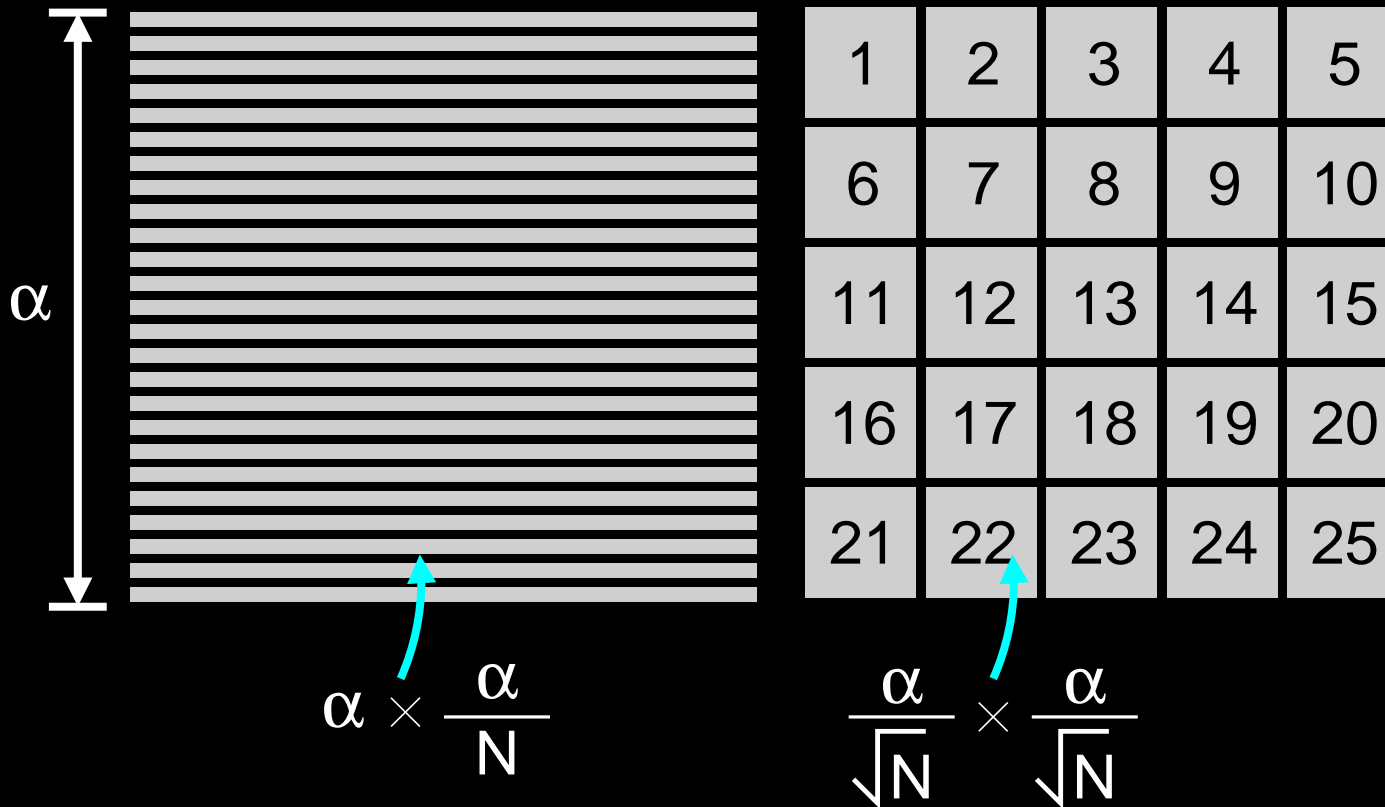
## - Part I

- Three floorplan alternatives for a crossbar NoC
- Why a centralized crossbar

## - Part II

- Centralized crossbar NoC design & numerics

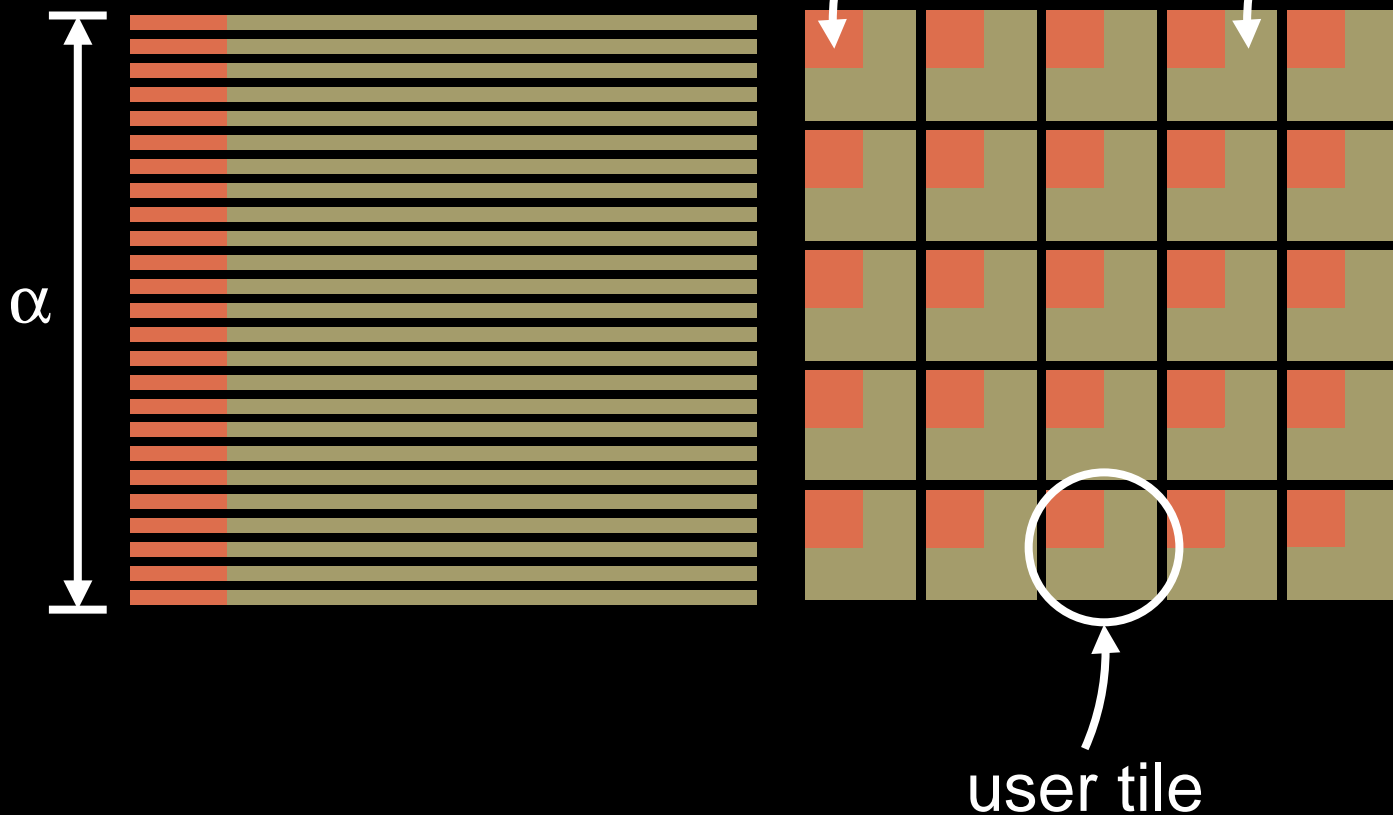
# Floorplan Alternatives for an example 25x25 Crossbar NoC



# Floorplan Alternatives for a 25x25 Crossbar NoC

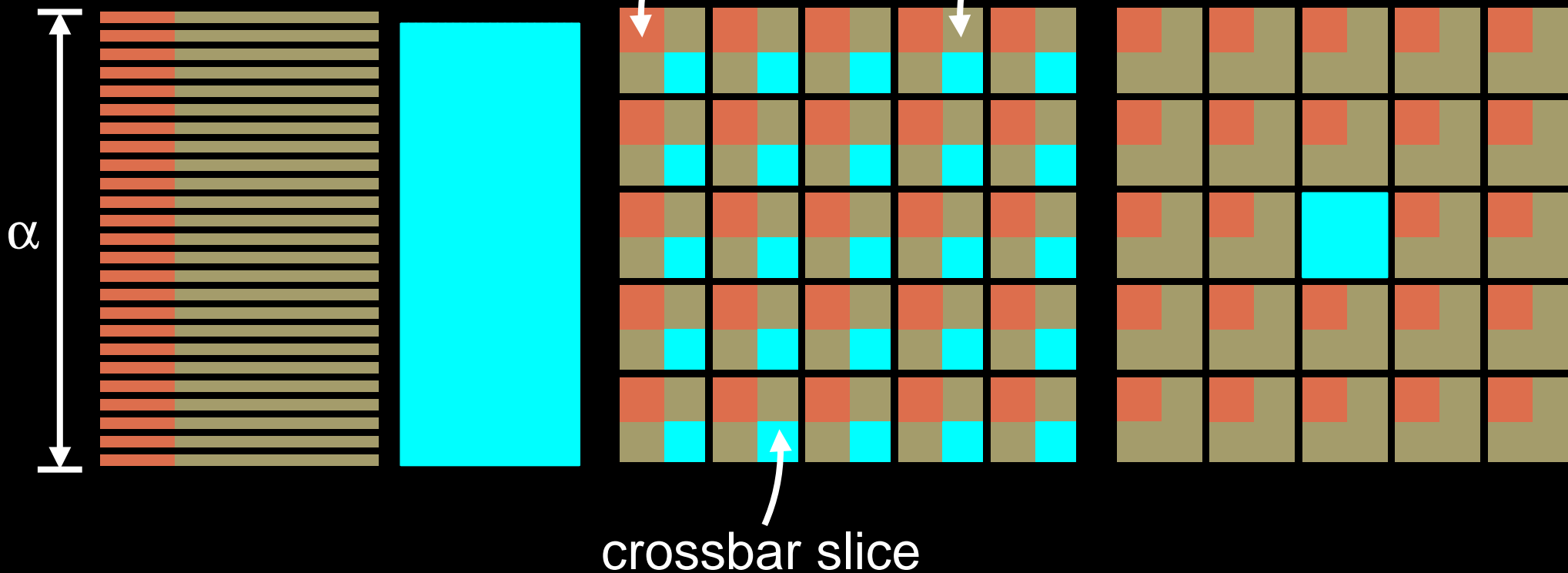
processor / switch–port control

memory / switch queues



# Floorplan Alternatives for a 25x25 Crossbar NoC

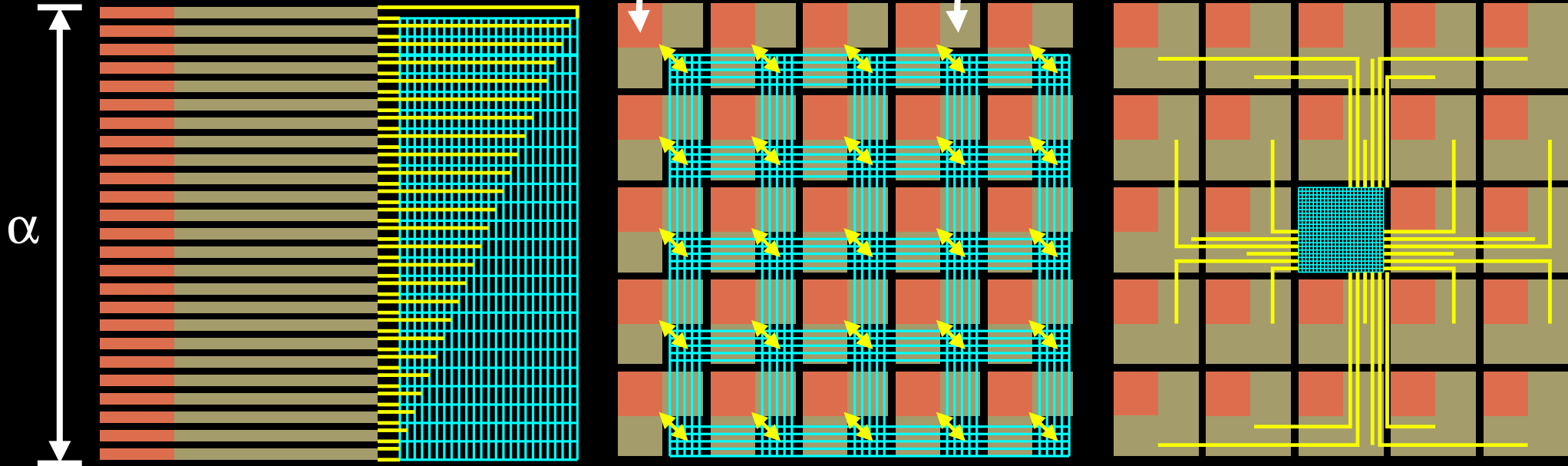
processor / switch–port control      memory / switch queues



# Floorplan Alternatives for a 25x25 Crossbar NoC

processor / switch-port control

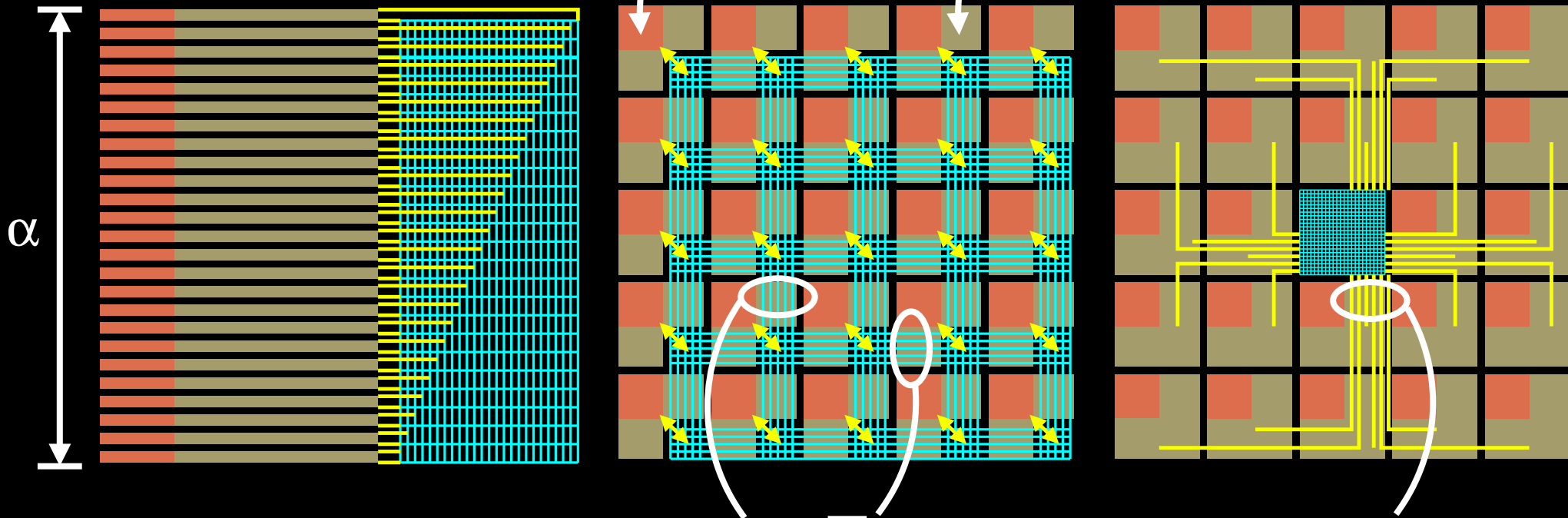
memory / switch queues



# Floorplan Alternatives for a 25x25 Crossbar NoC <sup>7</sup>

processor / switch–port control

memory / switch queues



# lines on top of memory:  $5 (= \sqrt{N})$

$12 (= 2 \times N/4)$

& total line length:  $50\alpha (= 2N\alpha)$

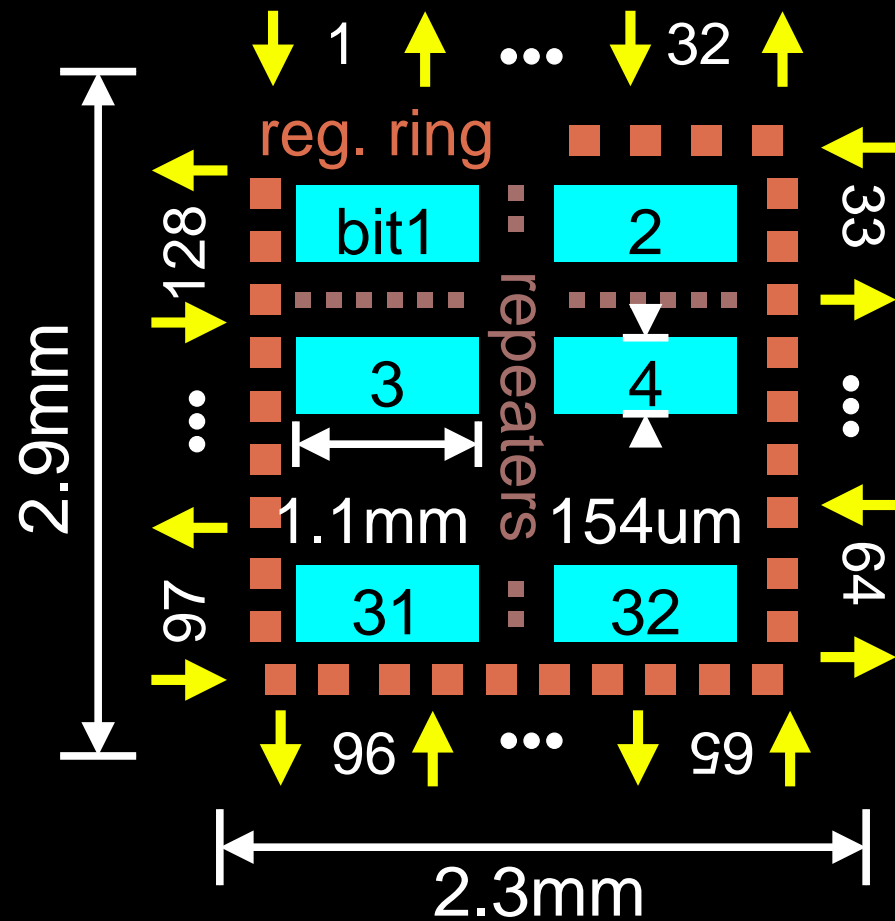
$25\alpha (= N\alpha)$

These are floorplans for a 25x25, not a 5x5 crossbar

# 128x128x24Gb/s Centralized-Crossbar Bit Slice

- 90nm CMOS standard cell, M1-M9
- Wide array of 128 128-to-1 quad-tree muxes
  - 1.1mm x 154um
  - 95% area utilization
- Routing in M2-M4
  - above the multiplexor standard cells
- 750MHz worst-case

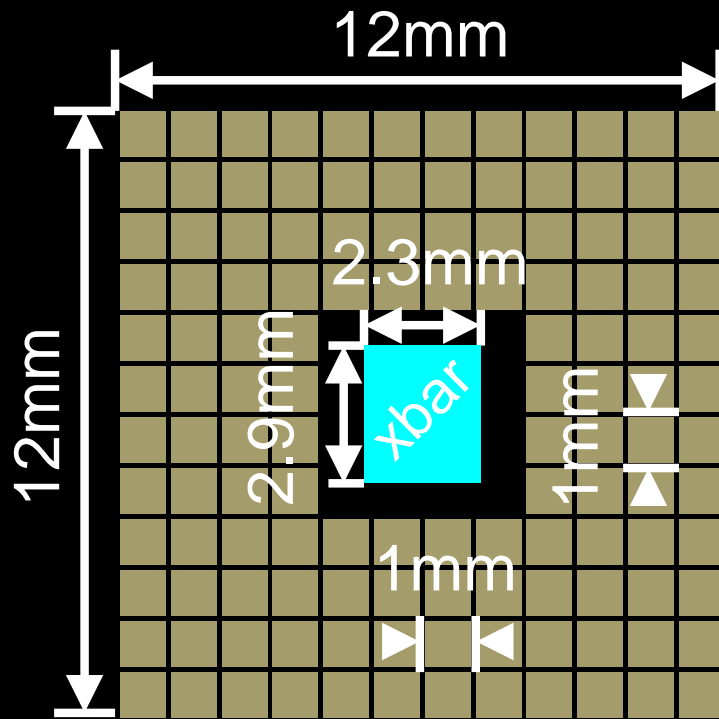
# 128x128x24Gb/s Centralized-Crossbar Floorplan



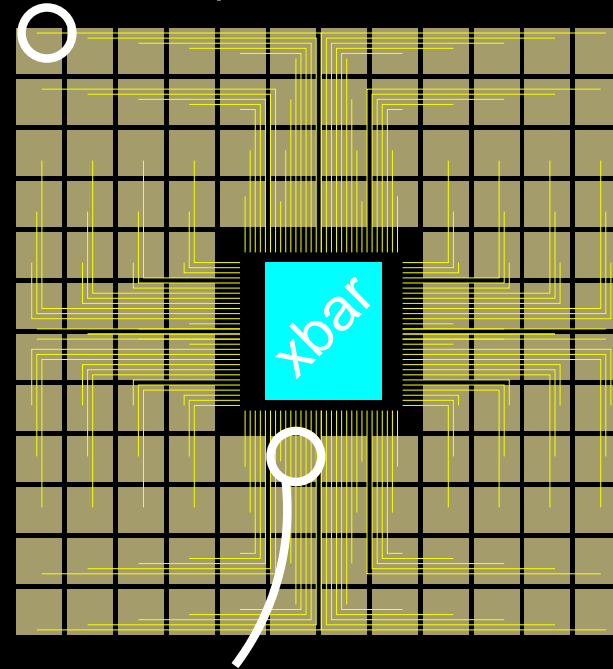
90%  
area utilization

- 32 bits @ 750 MHz → > 20Gbps port capacity
- IO needs to be routed to the slices
  - routing in M5-M8 (above the bit slices)
  - max wire length = half perimeter < 6mm
  - 6mm = max pipelined-link length @ 750MHz

# 128x128x24Gb/s Crossbar-NoC Floorplan



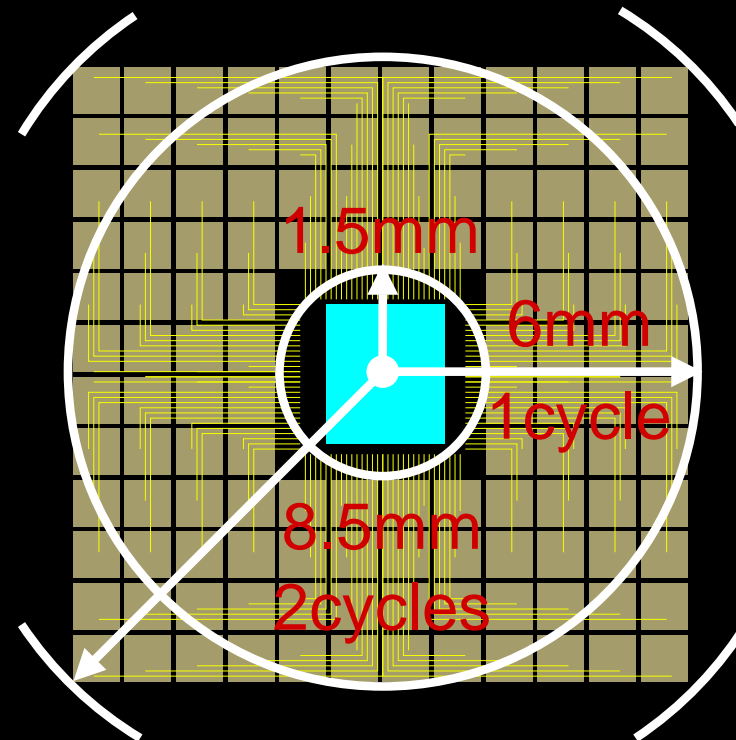
1 bidirectional 64-bit link  
M5-M6 (SRAM:M1-M4)



$8 \times 64 = 512$  metal tracks  
x 512nm routing pitch  
= 0.26mm = 1/4 x tile edge

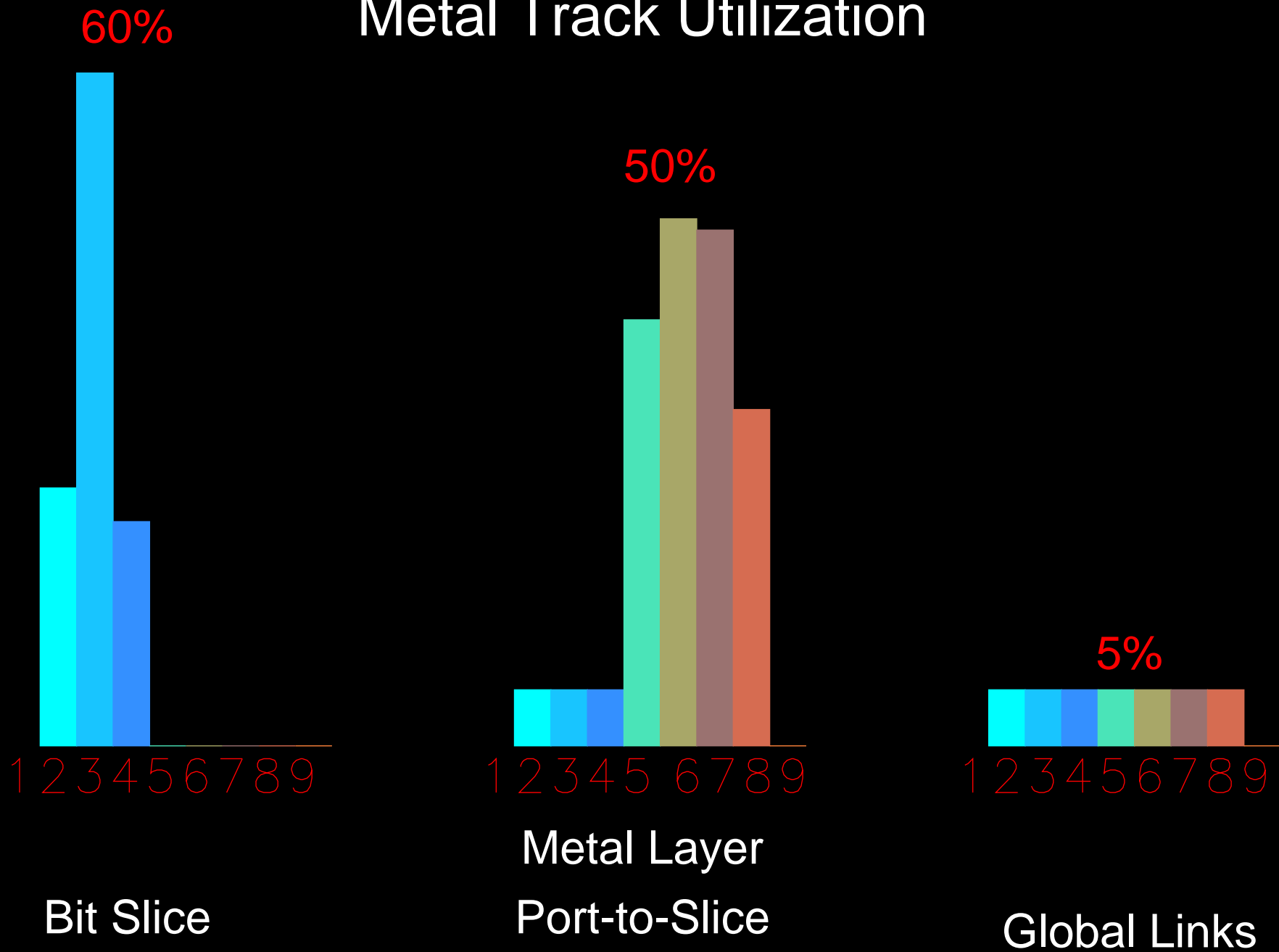
9 sq-mm left for centralized control

# 7-Cycle Corner-to-Corner Latency



- 2 cycles corner to center (crossbar port)
  - 1 cycle crossbar port to slice
  - 1 cycle slice in to out
  - 1 cycle slice out to crossbar port
- 2 cycles crossbar port (center) to to corner

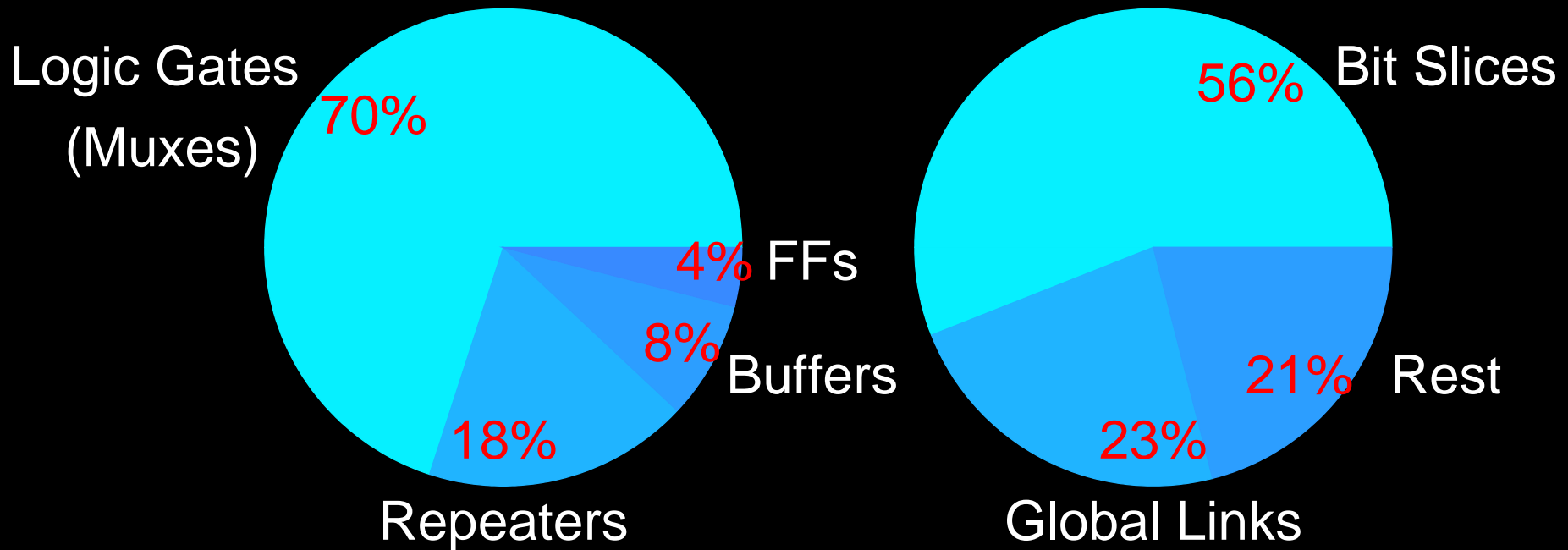
# Metal Track Utilization



Still plentiful of wiring resources not utilized

Std-Cell Area  
6.6 sq-mm

Power  
9 Watts



Traffic: Permutation updated / cycle - toggle rate = 1

Worst-case conditions: 0.9Volts, 750MHz

-- THE END --