Hierarchical Network-on-Chip for Embedded Many-Core Architectures

Alexandre GUERRE
DRT/DACLE/LCE
alexandre.guerre@cea.fr
Embedded Systems Context

- Embedded systems must support various applications
- They need more computing power and support dynamic applications
Solution and new problem

• Different solutions are used to provide high computing power
  ▪ One core with several IPs
  ▪ Many processors

• Regardless of the chosen solution, it is necessary to connect many processing elements and memories

• Dynamic applications forbid communication predictions
  ▪ Off-line mapping is not optimal in this case

• Those constraints require the interconnection to be scalable and to offer good performance for unpredictable traffic in the worst case

• Embedded computing adds area and power constraints
NoC solution

- Networks-on-chip are a suitable solution but many parameters have to be chosen (topology, buffer size...)

- Most of them are studied in different papers but no paper proposes area, power and performance studies on a wide range of topologies

- Our study proposes a performance and area exploration in the case of a many-core systems with a dynamic control
  - Power consumption is not considered

- We consider wormhole strategy, small buffers for network router and the simplest possible routing technique for each topology
Studied network topologies

- Multi-Bus
- 2D torus
- Butterfly multistage
- 2D mesh
- 4 clusters 1 link MultiRing
- 16 clusters 1 link CrossRing
- 9 clusters 2 link MultiTorus


**Study Environment**

- **Performance evaluation environment**
  - SystemC simulator
  - 256 traffic generators and 256 memories
  - Transaction Level Modeling (customized TLM library)
  - Traffic generators, used to be able to change easily the network load
  - Two traffic models
    - Random traffic (no mapping strategy)
    - Local traffic (smart mapping on the system)

- **Area synthesis environment**
  - Based on VHDL code
  - 256 inputs and outputs
  - Synopsys Tools, used to obtain area post synthesis
  - TSMC 40 nm
- Torus topology presents the best performance
- Hierarchical networks have average performance

- Increase of the Hierarchical networks performance
- Same for Torus and Mesh but with a smaller ratio
Area results

- Area for 256 input/output network

Hierarchical networks consume less area
Area efficiency results

- New comparison: the load of each network is divided by the area of the network

Uniform traffic

Local traffic

MultiCross and MultiTorus obtain the best area efficiency
Conclusions and future work

- Hierarchical networks allow less area consumption
- Higher radix router allows also area decrease
- MultiCross topology is the smallest and the MultiTorus topology offers the highest performance
- MultiCross is the most area efficient
  - The switch in the router is used as an intermediate hierarchical level
- Power consumption study needs to be done
- This study is the first step for a definition of a many-core architecture which supports dynamic applications